DESIGN FOR ELECTROSTATIC-DISCHARGE (ESD) PROTECTION IN TELECOMMUNICATIONS PRODUCTS

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Electrostatic discharge (ESD) can seriously damage electronic devices and affect the operation of the systems that contain them. Today, design for ESD protection has become a critical—and more difficult—consideration because of shrinking device feature sizes, high system operating speeds, factory automation, and the growth of uncontrolled user environments. To meet this challenge, designers must consider ESD protection early in the product-development process. The designer must also work with the factory engineer to identify performance and manufacturing process tradeoffs and assess their relative importance. Also, testing to customer requirements should be done early and often during the development process. This paper describes ways to limit the damaging effects of ESD at the device, circuit-pack, and system levels. As an example of device-level ESD-protection schemes, we present an approach employed at AT&T Microelectronics. We also review product testing for ESD, industry test standards, and future trends.

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Introduction

The term *electrostatic discharge* (ESD) refers to the sudden transfer of charge between objects at different electrostatic potentials. A familiar example is the "zap" (arc discharge) you feel after walking across a synthetic carpet on a dry day and then touching a metal door knob. This seemingly insignificant event can have serious, harmful effects on microelectronic devices and the equipment that contains them. For example, for a person to feel it, an ESD event must involve a minimum electrostatic potential of about 3 kV (kilovolts). The energy transferred will be several hundred microjoules. If an integrated circuit (IC) is in the path of this discharge, a current of several amperes will flow through the circuit's tiny silicon junctions, gate oxides, and

Panel 1. Acronyms and Terms in This Paper

ANSI	American National Standards Institute	MOSFET	metal-oxide semiconductor, field-effect transistor
CDM	charged-device model	NMOS	n-channel metal-oxide semiconductor
FCDM	field-induced charged-device model	n^+	heavily doped material in which electrons carry the current
CISPR	International Specification Committee on Radio Interference	n^-	lightly doped material in which electrons carry the current
CMOS	complementary metal-oxide semiconductor	npn	adjacent layers of n-type, p-type, and n-type materials
DIP	dual in-line package	p^+	heavily doped material in which holes carry the current
EMI	electromagnetic interference	p^-	lightly doped material in which holes carry the current
EOS	electrical overstress	pn junction	juncture of p-type and n-type materials
ESD	electrostatic discharge	PVC	polyvinylchloride
EUT	equipment under test	PWB	printed-wiring board
HBM	human-body model	RC	resistance-capacitance
IEC	International Electrotechnical Commission	Si_3N_4	silicon nitride
IEEE	Institute of Electrical and Electronics Engineers	UV	ultraviolet
LARC2	layout rule checker	VLSI	very-large-scale integration
LDD	lightly doped drain		
MIL STD	military standard		
MOS	metal-oxide semiconductor		

interconnections. This is more than enough to cause melting or dielectric breakdown in an unprotected device. If the discharge is to an operating electronic system. a variety of malfunctions can occur, in addition to the possible hardware damage. Radiation from the discharge can induce voltages on signal paths, which cause bit errors, loss of memory, dropped calls, false alarms, or even system shutdown. Unfortunately, in the last ten years, these effects have been observed many times throughout the electronics industry and have been the cause of serious manufacturing yield losses, equipment malfunctions, and lost revenue. (Panel 1 defines acronyms and terms used in this paper.)

Approaches to Minimizing ESD. There are two parallel approaches to minimizing the effects of ESD. In this paper, we refer to these approaches as: control and designed-in protection.

Control refers to the materials and procedures that are employed in manufacturing and use environments to keep static potentials and discharge currents low. The most well-known element of ESD control is the grounding wrist strap that has become ubiquitous in circuit-assembly factories. Other controls include antistatic materials (to prevent triboelectric charging), air ionizers, and static-dissipative work surfaces. These controls and audits of them represent a major expense that is borne by the manufacturer or equipment user. The more sensitive a device or system is to ESD, the more stringent are the controls needed to ensure adequate yield and reliability.

While these controls can reduce the phenomenon to a manageable level, they by no means eliminate the problem. The ability of manufacturers and customers to implement effective controls varies widely, and many

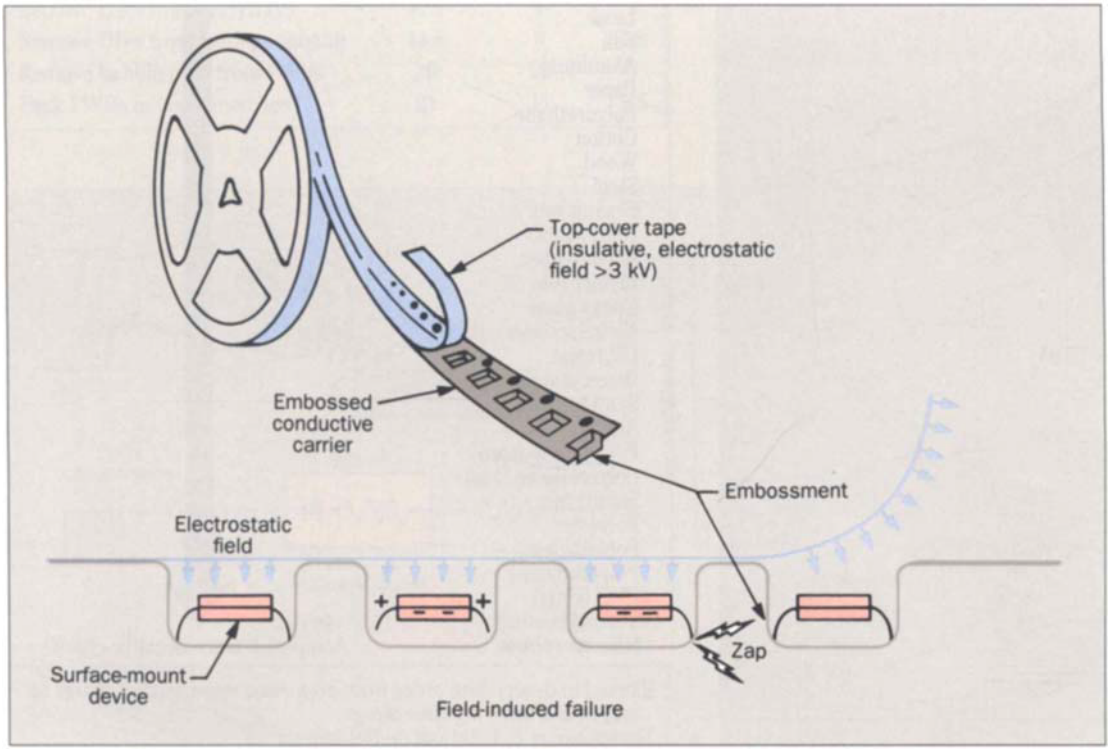


Figure 1. ESD concerns raised by tape-and-reel packaging. Random motion in a tape-and-reel carrier tape or the electrostatic field on the cover tape may charge a device, and a field-induced failure may occur.

customers would like to minimize or, sometimes, eliminate the expense associated with these controls. Even in the best of factories, ESD failures occur when very sensitive components appear in the factory without adequate warning. In some applications, such as a business customer's office, ESD controls are often impractical. Telecommunications equipment users are also concerned about the potential latent effects of ESD. These occur when an ESD failure is not detected before the device is shipped, or ESD weakens a device enough to cause an early field failure. Because of these concerns, *designed-in ESD protection* has become an important product attribute.

In the electronics industry, the current state of affairs regarding ESD is a tenuous balance between control and protection. If technology were not changing at a rapid pace, one might assume that the ESD problem had been conquered. However, two important trends have already begun to upset this balance:

- Customers are demanding higher speed and performance from integrated circuits. This trend is driving IC designers toward higher scales of integration (smaller circuit features) and putting more stringent limits on input resistance and capacitance. This makes proper ESD protection difficult because effective protection circuitry, if not optimized, tends to be large and loads the device's inputs and outputs.
- Manufacturing is moving to various forms of automatic handling. In general, the implementation of ESD control lags behind this trend. An example is the move

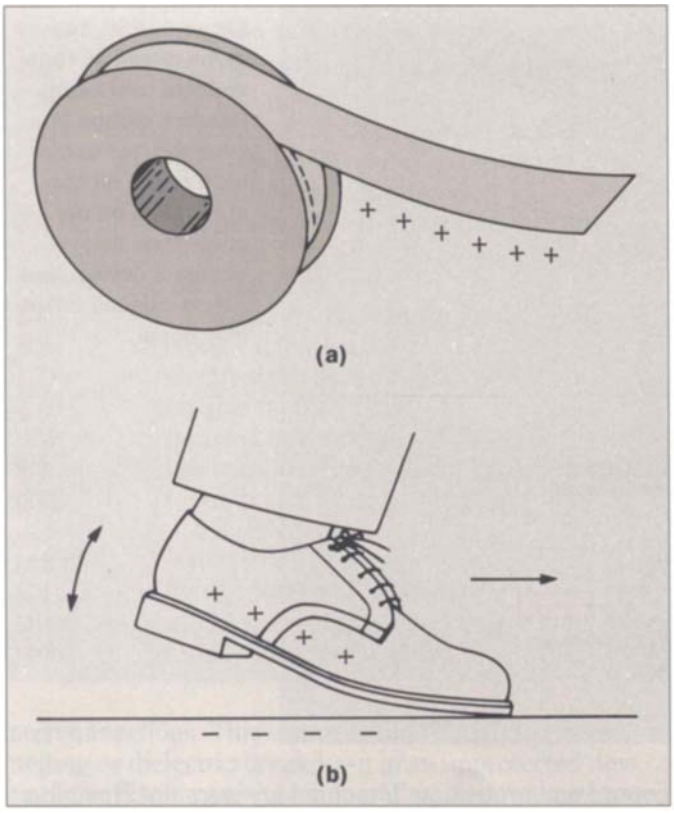


Figure 2. Common examples of static-charge generation. (a) The adhesive side of the cellophane tape picks up a positive charge as it is unrolled. (b) As the person walks across a synthetic carpet, his or her shoes gain a positive charge.

from shipping tubes to tape and reel (Figure 1) as the primary method for handling devices. Unless properly designed, tape-and-reel packaging machines can be efficient electrostatic generators.[1]

Clearly then, unless manufacturers and designers direct special attention to ESD control *and* protection, failures and malfunctions will increase in the future.

Table I. Triboelectric Series

Material*	Polarity (+ or –)
Asbestos	Acquires a more positive charge
Acetate	
Glass	
Human hair	
Nylon	
Wool	
Fur	
Lead	
Silk	
Aluminum	
Paper	
Polyurethane	
Cotton	
Wood	
Steel	
Sealing wax	
Hard rubber	
Acetate fiber	
Mylar† film	
Epoxy glass	
Nickel, copper, silver	
UV resist	
Brass, stainless steel	
Synthetic rubber	
Acrylic	
Polystyrene foam	
Polyurethane foam	
Saran† film	
Polyester	
Polyethylene	
Polypropylene	
PVC (vinyl)	
Teflon§ coating	
Silicone rubber	Acquires a more negative charge

* Ranked in descending order from *acquires a more positive charge* to *acquires a more negative charge.*
† Trademark of E. I. duPont de Nemours.
§ Trademark of Dow Chemical U.S.A.

Static Generation

A static charge is generated whenever two different materials come into contact and are then separated. Figure 2 illustrates two common examples: the charge generated on a person as he or she walks on a carpet, or generated on cellophane tape as it is unrolled. This phenomenon is called the *triboelectric effect* and has been known since the days of the ancient Greeks. However, we know surprisingly little about the underlying mechanisms that produce it.

We do know that some materials tend to charge positively, while others tend to charge negatively. The triboelectric series (Table I) summarizes this tendency.

Table II. Typical Electrostatic Voltages (in kV)

Event	Relative humidity		
	10%	40%	55%
Walking across carpet	35	15	7.5
Walking across vinyl floor	12	5	3
Motions of bench worker	6	0.8	0.4
Remove DIPs from plastic tubes	2	0.7	0.4
Remove DIPs from vinyl trays	11.5	4	2
Remove DIPs from foam packaging	14.5	5	3.5
Remove bubble pack from PWBs	26	20	7
Pack PWBs in foam-lined box	21	11	5.5

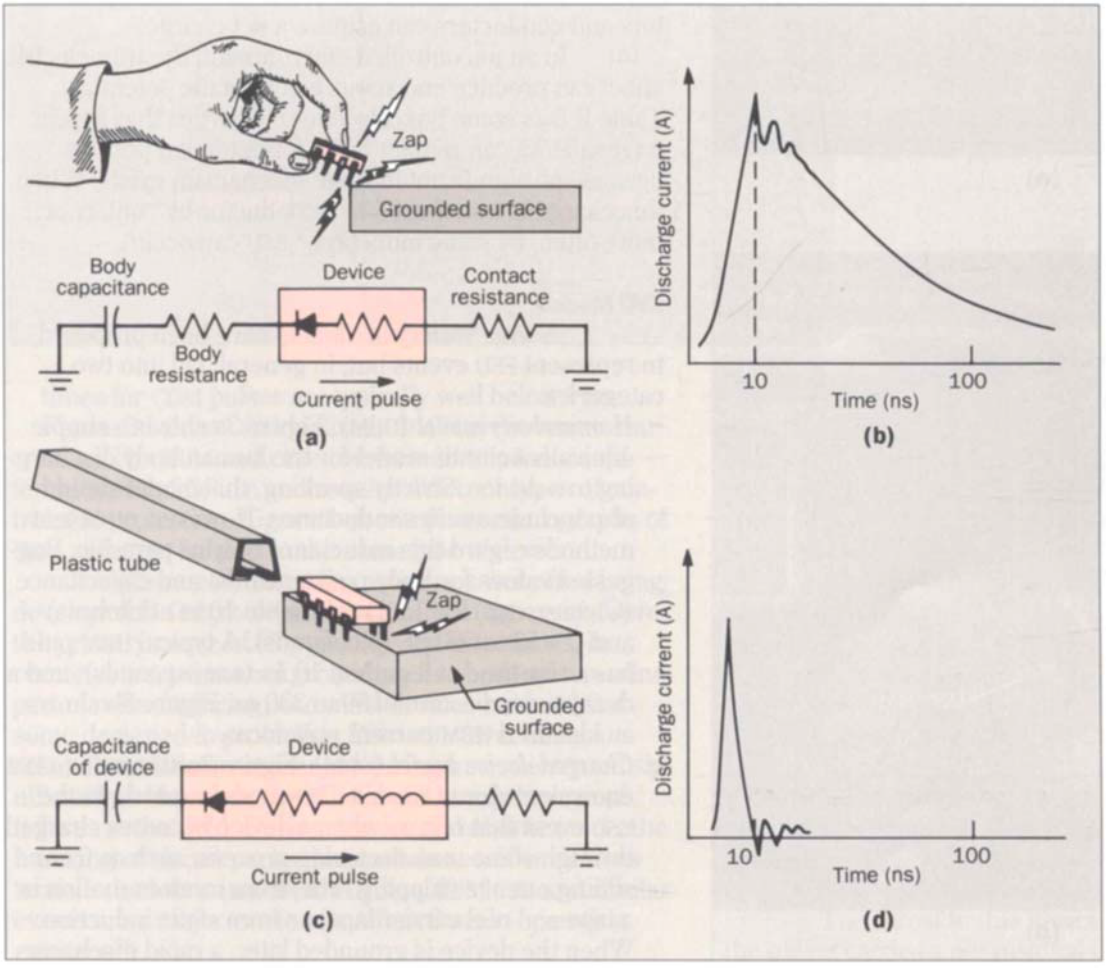
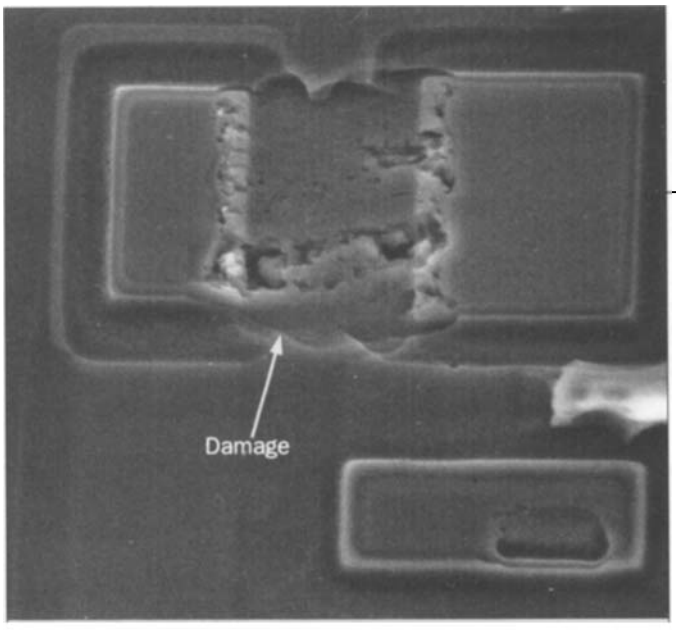
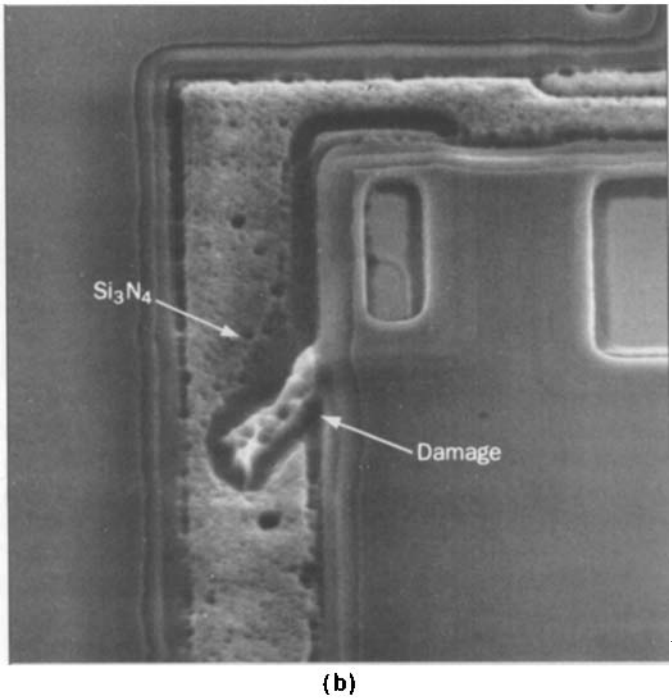


Figure 3. ESD models. (a) Equivalent circuit of the HBM. Resistance (R) may range from 150Ω to 10 kΩ, and capacitance (C) from 20 to 500 pF. (b) Idealized current waveform of the HBM. The pulse's rise time is typically less than 10 ns, and its decay time is between 50 and 300 ns. (c) Equivalent circuit of the charged-device model (CDM). The magnitude (resistance and capacitance) of the circuit elements depends on the device. (d) Idealized current waveform of the CDM. The pulse's rise and fall times are typically well below 1 ns.



(a)



(b)

Figure 4. ESD damage to a device. (a) HBM ESD causes silicon in the pn-junction area to melt. (b) CDM ESD causes dielectric breakdown of the (Si_3N_4) insulation.

A material at the top of the series will tend to charge positively with respect to materials below it. Both insulators and conductors can acquire a net charge.

In an uncontrolled environment, the triboelectric effect can produce enormous electrostatic potentials. Table II lists some typical values.[2] Charges that appear on insulators can remain there for extended periods because no significant leakage mechanism exists. When this charge is transferred to a conductor by contact or, more often, by static induction,[3] ESD can occur.

ESD Models

A wide variety of models have been proposed to represent ESD events but, in general, fall into two categories:

- *Human-body model* (HBM). Figure 3a shows a simple equivalent-circuit model for the human body discharging to a device. Strictly speaking, this model should also include a series inductance. However, most test methods regard this inductance only as parasitic. Suggested values for body resistance (R) and capacitance (C) vary, e.g., R = 150Ω (ohms) to 10 kΩ (kilohms) and C = 50 to 500 pF (picofarads). A typical HBM pulse has a rise time of less than 10 ns (nanoseconds), and a decay-time constant of 50 to 300 ns. Figure 3b shows an idealized HBM current waveform.
- *Charged-device model* (CDM). Figure 3c shows the CDM equivalent-circuit model. This model represents the ESD event that occurs when a device becomes charged through some manufacturing process, such as from sliding out of a shipping tube, from random motion in a tape-and-reel carrier tape, or from static induction. When the device is grounded later, a rapid discharge occurs. The discharge current is limited only by the device's parasitic impedance. As a result, rise and fall

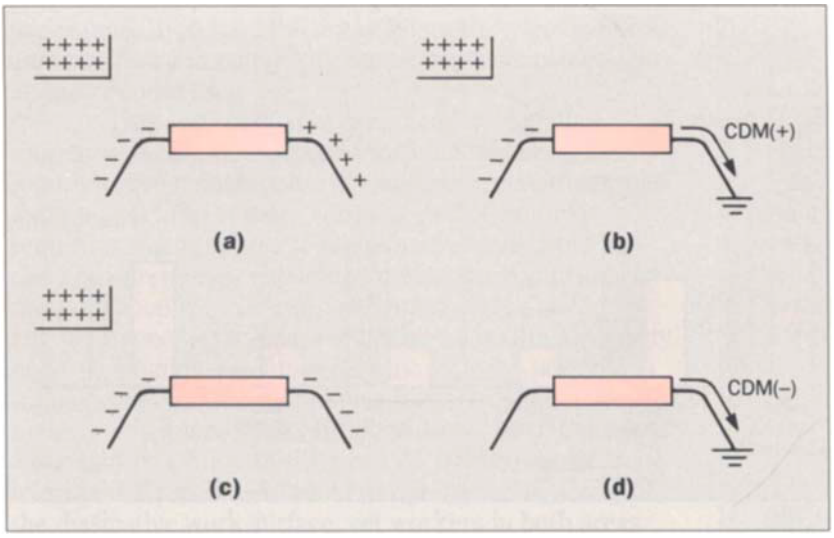


Figure 5. ESD by static induction and double jeopardy. (a) A neutral device is placed near a positive static charge, which causes a charge separation on the device-lead frame. (b) First ESD event, a lead is then grounded. A charge with the same polarity as the static field is driven to the ground. (c) The device is left with a net charge. (d) Second ESD event, grounding in a later production step. Charge transferred is equal in magnitude to the first event but of opposite polarity.

times for CDM pulses are typically well below 1 ns. Figure 3d shows an idealized CDM current waveform.

The HBM and CDM events tend to produce different types of failure and require different types of control and protection. Figure 4 shows photomicrographs of HBM and CDM failures in the same type of device.

When manufacturing processes were first being developed for microelectronic circuits, HBM events were the primary cause of ESD yield losses in factories. In recent years, personnel grounding has become a routine part of manufacturing, and most devices have at least some designed-in protection from HBM events. As a result, HBM failures in manufacturing have decreased significantly.[4] However, the HBM is still a major cause of failures in the field. During service and maintenance, the handling of circuit packs that contain sensitive devices tends to be less controlled. Further, HBM ESD and similar events are a major cause of malfunctions in operating equipment.

On the other hand, because of the rapid changes that are occurring in circuit-assembly procedures, the CDM is just emerging as a significant ESD concern.[1,5–8] Many new processes are being introduced into factories without adequate regard for static generation. Improperly designed or installed conveyor belts, slides, robotic arms, or test equipment can systematically damage CDM-sensitive devices.

Static Induction. One particularly subtle but common way that CDM occurs is by static induction.[1,3] Figure 5 illustrates this series of events.

In this process, a neutral object (such as an IC) is placed near a static charge that resides on an insulator in the work area. The field from this static charge will cause (induce) a charge separation on the lead frame and conductors of the device. If a device lead is subsequently grounded, a potentially damaging current will flow. These charges, which have the same polarity as the static charge, are driven to ground by the field.

The threat to this device does not end there. Now, the object carries a net residual charge. The charge remains until it dissipates into the air (which may take minutes or hours), or until the device is grounded in a

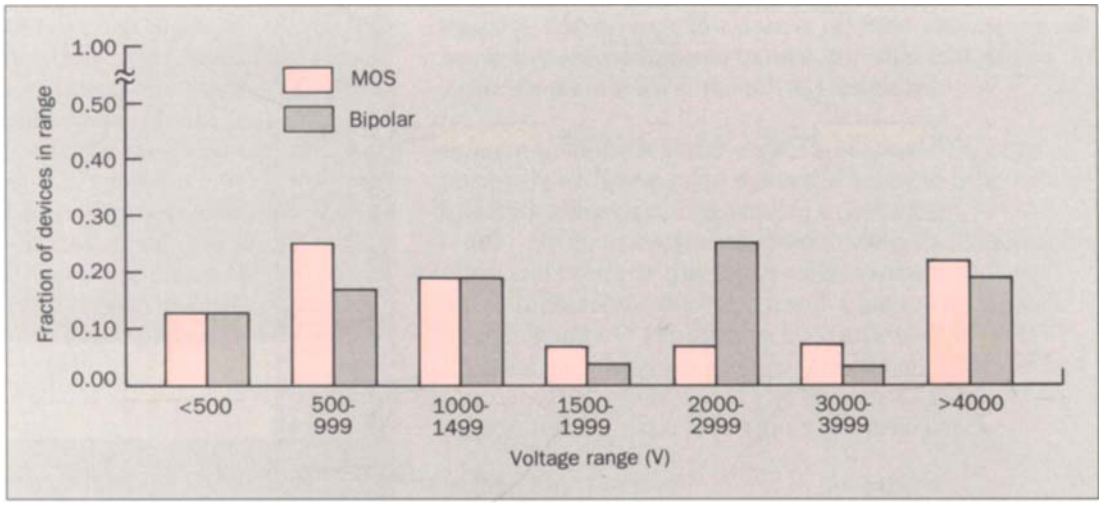


Figure 6. HBM ESD withstand thresholds for MOS and bipolar devices. Technology is a weak indicator of device sensitivity.

subsequent process step. If the latter occurs, the result is a second event, opposite in polarity and equal in magnitude (charge) to the previous one.

Sensitivity to ESD. The HBM and CDM models are used as the basis for standard test methods for characterizing devices and systems. We customarily express a device's relative susceptibility to ESD in terms of the voltage that appears on the capacitor in these models. We define a device's *withstand threshold* as the highest voltage it is known to withstand without changing its operating characteristics. Microelectronic devices range in sensitivity from about 20V (volts) for unprotected MOS (metal-oxide-semiconductor) transistors, to greater than 1.5 kV for some Zener diodes.

MOS was an early focus of ESD protection because of the inherent sensitivity of the thin gate oxide (less than 1000 angstroms). It became popular to say that MOS integrated circuits were more sensitive than bipolar devices. However, data collected recently by the military suggests that device technology is a poor indicator of device sensitivity (Figure 6). Therefore, it is important to test all new device designs for their HBM and CDM sensitivity, so that proper handling precautions can be applied.

ESD Control in Manufacture

AT&T facilities use the ESD-control program described in AT&T's *Electrostatic Discharge Control Handbook*.[2] The overall program consists of the four main elements in Panel 2, which emphasize realistic requirements and avoid expensive overkill. Manufacturing locations use these elements to verify that their programs meet customer expectations. In addition, major telecommunications equipment customers routinely audit our compliance to this program.

Three basic rules (also listed in Panel 2) apply regardless of device sensitivity. Additional requirements are added to this list as a function of device sensitivity. Less sensitive products require minimum precautions at minimum cost. On the other hand, the requirements for ultrasensitive devices specify more extensive precautions and are based on an area-sensitivity classification system (Tables III and IV). This system is similar but not identical to the classification systems specified by military standards (MIL STDs).[9]

In a manufacturing facility, an area's classification (Class 0 through Class IV) is governed by the most sensitive device to be handled in that area. Thus, circuit

packs (and, therefore, the areas where they are handled) are classified according to the most sensitive component on the circuit pack.

This system of area classification simplifies training and communications for a manufacturing facility. It permits the manufacturer to engineer greater control into the handling of more sensitive devices without requiring its employees to learn more complicated handling requirements. The added protection is provided by using ESD-control materials and equipment. The factory engineer specifies this protection based on the sensitivity of devices handled in the area. This makes it possible to train employees with techniques that are common to all areas. For instance, Class III areas do not use dissipative work surfaces, but Class II areas do. Therefore, the devices in the Class II area are better protected by virtue of the dissipative work surface, yet workers in both areas follow the same handling procedures.

Besides the progressive precautions that are described in Table IV, some additional requirements have recently been developed at AT&T for handling and shipping devices:

- Shipping tubes may not be used to handle or ship any device that has a CDM withstand threshold below 200V (Class 0).
- Tape-and-reel packaging may not be used to handle or ship any device that has a CDM withstand threshold below 1 kV on its corner pins or 500V on other pins, unless certain special materials are specified.

These requirements emphasize the need for ESD withstand-threshold information.

Class 0 devices present special problems not explicitly identified in Table IV. Devices this sensitive usually require treatment specific to the device and the manufacturing process.

Designed-In Protection

Considerable effort is required to minimize ESD effects in manufacturing. However, any control program would largely be ineffective if some protection were not built into the devices being handled. Without specific protection circuitry, MOS devices would all be Class 0, and large-scale manufacturing would be extremely expensive, if not impossible.

Further, once the devices leave the factory in assembled circuit packs, an entirely new set of threats appears in installation, maintenance, and service. Usually, someone other than the equipment manufacturer performs these functions. Thus, additional protection is required to survive this more hostile environment. Because performance requirements may limit the on-chip protection of some devices, protection may also be required at the circuit-pack or system level.

Another major ESD design concern is the protection of systems from upset caused by the radiated effects of ESD. The inability of equipment to operate reliably when an operator approaches or touches it is a serious

Panel 2. AT&T ESD Control Program

Main Program Elements:

- Demonstrable compliance with the policies and procedures in AT&T's *Electrostatic Discharge Control Handbook*.[2]
- An auditing program based on AT&T's ESD inspector's guide, or equivalent.
- A formal manufacturing acceptance procedure for verifying that designs comply with appropriate standards.
- Documentation and personnel awareness of manufacturing area classifications and procedures.

Basic Rules (applied regardless of device sensitivity):

- Assume that all electronic (solid-state) components and assemblies are sensitive to ESD damage.
- Never touch a sensitive component or assembly unless you are properly grounded.
- Never transport, store, or handle sensitive components or assemblies expect in a static-safe environment.

Table III. Area Sensitivity Classification

Class	Sensitivity
0	Area contains devices with ESD withstand thresholds that range from 0 to 199V
I	Area ranges from 200V to 499V
II	Area ranges from 500V to 1.999 kV
III	Area ranges from 2 kV and above
IV	Area does not contain devices that are sensitive to ESD damage

product deficiency. This is especially important for office and consumer products, whose user environments usually do not include any ESD controls.

A comprehensive description of ESD protection from hardware damage and equipment malfunction is beyond the scope of this paper. Instead, we give some brief illustrations of protection at the device (e.g., integrated circuit), circuit-pack, and system levels.

Devices. To achieve ESD protection of devices, special protection circuits are placed next to each pin on an integrated circuit. These protection circuits absorb the discharge without damage to themselves or to the circuits they protect. The types of protection used depend on the device technology and the fabrication process.

Here, we describe the protection scheme used in CMOS (complementary metal-oxide-semiconductor) devices designed and manufactured by AT&T Microelectronics. Descriptions of other protection schemes have been published elsewhere.[8,10–13]

Today, CMOS is the technology of choice for most VLSI (very-large-scale-integration) devices because CMOS circuits consume little power, compared to bipolar or NMOS (n-channel, metal-oxide-semiconductor) devices. The primary ESD failure modes of CMOS components are:

- Breakdown of the thin oxide in the MOS structure.
- Leaky pn junctions. (This is the junction formed at the joining surface of a p-type material and an n-type material.)
- Dielectric breakdown.
- Fusing of conductors.

As VLSI devices are scaled down, the thin oxide becomes thinner [15 nm (nanometers) in state-of-the-art devices] with lower breakdown voltages. Junctions become shallower and more prone to degradation. Dielectrics become thinner. Conductor lines are narrower and, therefore, more susceptible to fusing. Thus, the task of protecting the circuits against ESD becomes more challenging.

Protection schemes. Figure 7a shows a typical CMOS input-protection circuit. Dual diodes connected directly to the bond pad are the primary protection devices. The diode D1 to V_{ss} provides the discharge path for negative pulses, and the diode D2 to V_{dd} conducts during positive pulses. The resistor, along with the gate capacitance, provides an RC (resistance-capacitance) delay that slows the charging of the gate. Additional dual diodes (D3 and D4) provide fast discharge paths for the gate charge (particularly useful for CDM protection).

Figure 7b shows the layout of the input protection circuit. The primary diodes (D1 and D2) are laid out around the bond pad to distribute the current evenly and minimize the area consumed by the protection device.

CMOS output circuits (Figure 7c) are protected by virtue of the parasitic drain-to-well diodes D1 and D2, associated with the CMOS process. [*Drain* and *well* refer to specific parts of the CMOS structure. An unintentional (parasitic) diode may exists between them, which happens to be useful.] The n-channel pull-down device contains the n^+/p-well diode D1, and the p-channel pull-up device inherently includes the p^+/n-well diode D2. These diodes are not optimized to conduct large currents, especially for slow or small drivers. So, an additional set of diodes is placed around the bond pad (Figure 7d).

Because the advanced CMOS processes now use a lightly doped drain (LDD) and silicided source and drain, the output buffers are becoming more sensitive to ESD.[14–16] Here, failures usually occur in the n-channel driver and are either the result of thin-oxide damage or

Table IV. Minimum ESD Control Techniques Specified by Class

Control technique	Area classification* (Device sensitivity) 0 (0-199V)	I (200-499V)	II (500-1999V)	III (2+ kV)	IV (None)
Personnel awareness/training	R	R	R	R	—
Auditing compliance to ESD	R	R	R	R	—
Personnel/facility certification	R	R	R	R	—
Personnel grounding	R	R	R	R	—
Carts	R	R	R	R	—
Static-safe packaging	R	R	R	R	—
Static-safe bags	R	R	R	S	—
Dissipative mats, tabletops	R	R	R	S	—
Conductive goldfinger shunts	R	R	R	S	—
Static-safe tubes	X	R	R	S	—
Static-safe tote boxes	R	R	S	S	—
Dissipative floor/finish	R	S	S	S	—
Extraordinary measures†	R	S	S	S	—
Other controls (as required)					
Air ionizers	S	S	S	S	—
Antistatic smocks	S	S	S	S	—
Conductive packaging	S	S	S	S	—
Conductive foam	S	S	S	S	—

* R = always required when used; S = may be specified by Engineering to provide additional protection from unusual hazards; X = tubes are not permitted for Class 0 devices.
† Stringent controls specifically designed for a given application.

degradation of the n^+/p-well junction. The cause of the damage is thought to be a secondary breakdown following "snap back" of the parasitic npn device. [This npn device is associated with the n-channel MOSFET (metal-oxide-semiconductor, field-effect transistor).] A similar, lateral npn (or snap-back) device that does not have a thin oxide is placed between the bond pad and V_{ss} to help protect the output buffer.

On-chip ESD-protection audit. Before a device design is complete and submitted to the mask-making shop, an automatic layout audit is done by a program called LARC2 (layout rule checker). ESD layout rules are part of this audit. For example, LARC2 checks for:

- A contact between the bond-pad metal and n^+-type silicon. This ensures that at least one diode (n^+/p-well) is connected directly to the pad. (For some applications, bond-pad contact is permissible only with that type of diode.)
- A minimum spacing of 2.5 μm (micrometers) between a pad metal and any other metal. This rule was

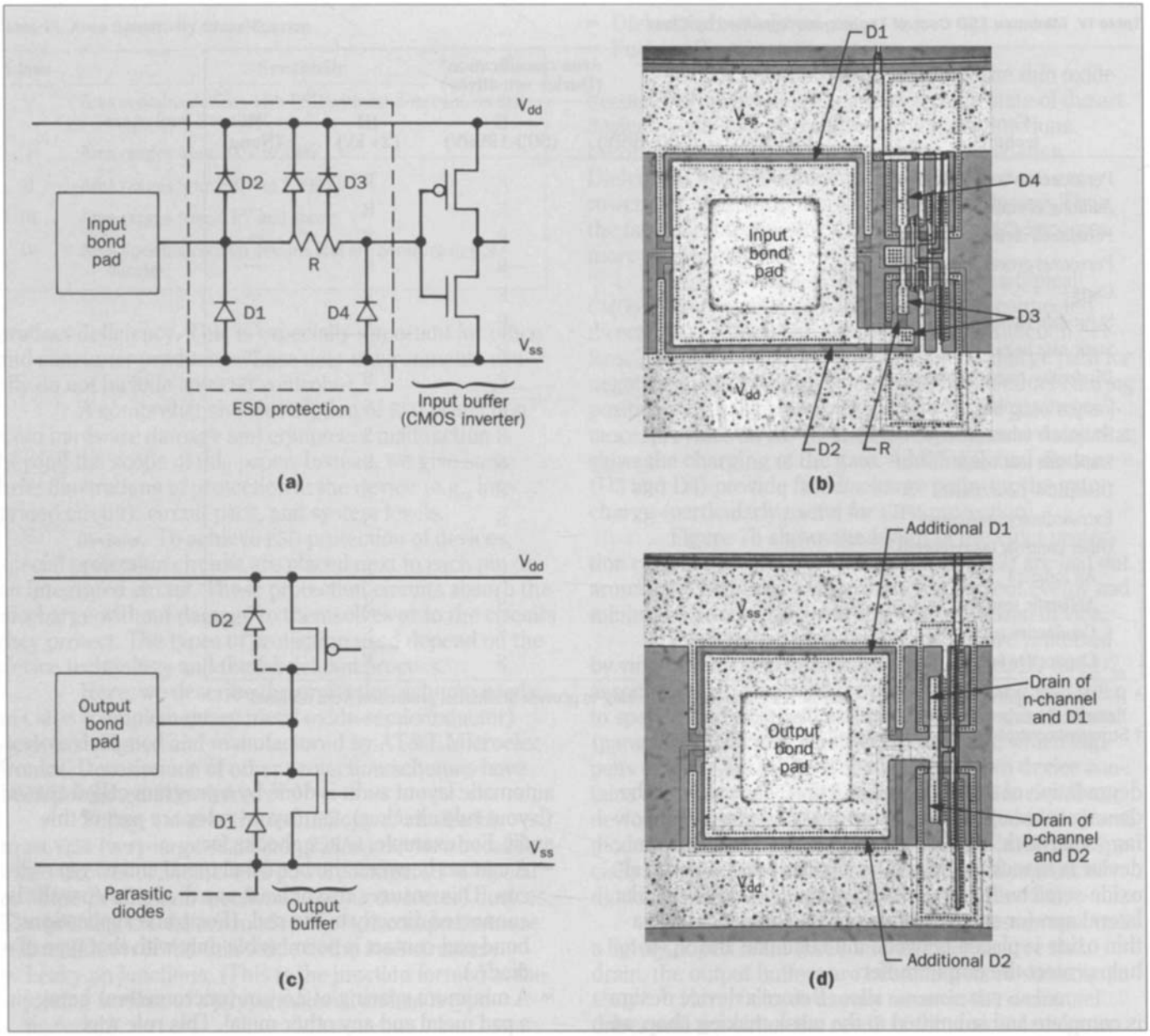

Input bond pad
D2
D3
R
D1
D4
V_{dd}
V_{ss}
ESD protection
Input buffer (CMOS inverter)
(a)
D1
V_{ss}
D4
Input bond pad
D3
V_{dd}
D2
R
(b)
V_{dd}
D2
Output bond pad
D1
V_{ss}
Parasitic diodes
Output buffer
(c)
Additional D1
V_{ss}
Drain of n-channel and D1
Output bond pad
Drain of p-channel and D2
V_{dd}
Additional D2
(d)

Figure 7. Typical CMOS protection circuits. (a) CMOS input buffer with its ESD protection. D1 discharges negative pulses and D2 conducts positive charges. Additional dual diodes, D3 and D4, provide discharge paths to V_{dd} and V_{ss}. (b) The input buffer's primary diodes placed around the bond pad distribute current evenly and minimize the area needed for the protection circuit. (c) CMOS output buffer. Protection is provided by parasitic drain-to-well diodes D1 and D2. (d) The additional diodes are arranged around the output bond pad to increase current-carrying capacity.

instituted to avoid the possibility of a lateral dielectric breakdown.

Circuit Packs. Proper ESD design at the circuit-pack level must consider two different issues: protecting the sensitive components on the circuit pack from permanent damage, and minimizing operational upsets that are caused by radiated electromagnetic waves.

Pack and Component Protection. Contrary to popular belief, devices usually do not become less susceptible to ESD failures when they are placed on circuit packs. In fact, they may become more susceptible. Most protection for devices is provided primarily to enable them to withstand manufacturing and handling procedures during processing and assembly. These procedures are usually done in an ESD-conscious environment where proper ESD-control procedures can be systematically applied. Once the devices are placed on a circuit pack and shipped, they are no longer under the manufacturer's control. This is where the components may be most vulnerable to ESD damage. Field-failure data from Bell Communications Research[17] substantiates this. ESD and EOS (electrical overstress) have been identified as the causes of about 20 percent of the circuit-pack failures.

The protection of telecommunications-system circuit packs from ESD damage is a relatively new area. But as devices become more ESD sensitive, protection at the circuit-pack level will become more necessary. The following techniques can be used to improve the ESD robustness of circuit packs:

- Restrict access to connector terminals.
- Use decoupling capacitors wherever possible.
- Provide a perimeter guard ring connected to the appropriate ground return.
- Apply specific shielding and surge protection (diodes) to the most sensitive devices.
- Avoid the routing of sensitive leads directly to the connector or wiring side of the pack.
- Restrict access to device leads on the wiring side of the pack by using coatings or physical shields.

One final design technique that greatly affects circuit-pack susceptibility is proper *component selection.* Clearly, components that are least sensitive to ESD (i.e., they have the highest withstand voltages) should be selected whenever possible. Designers should take the time to gather this data. Special attention should be given to component substitutions, because functionally identical devices from different suppliers may have very different ESD withstand thresholds.

Effects of Radiation. Proper ESD design at the circuit-pack level can also reduce the effects of high-frequency radiation on system operation. Such radiation typically occurs when there is a discharge to a metallic housing or object near the circuit pack (e.g., face plates or latches).

Because this is an electromagnetic-radiation problem, basic EMI (electromagnetic interference) reduction techniques[18] should be used to minimize these effects. These techniques include:

- Use multilayer printed-wiring boards whenever possible.
- Use a perimeter guard ring to tie metal face plates and latches to the appropriate ground return.
- Use appropriate routing and power and ground planes or grids to minimize signal-to-ground and power-to-ground loops.

Systems. ESD design at the system level also seeks to avoid hardware damage from ESD and to minimize capacitive and inductive coupling of the ESD-generated electromagnetic field to the equipment. The best way to avoid both undesirable effects would be to

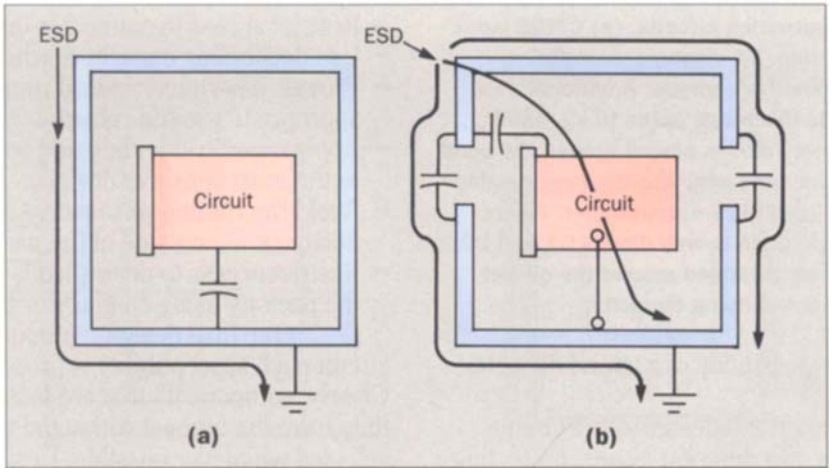


Figure 8. Metallic enclosures. (a) The Faraday shield completely encloses the circuit, directing currents and fields away from the circuit. When the shield is incomplete (b), a discharge can reach the circuit through seams, slots in the enclosure, or connection holes.

enclose the equipment completely in a Faraday shield (Figure 8a). Then, all currents and fields are directed away from the circuit. However, practical operations usually preclude such complete protection. Thus, a discharge can find its way to operating circuits through seams or slots in the enclosure and direct connections to the enclosure (Figure 8b).

In general, to reduce the effects of ESD, one should:

- Use shielded cables.
- Use common-mode chokes when necessary.
- Ground all exposed metallic components of a system.
- Minimize all physical openings in covers and doors.
- Seal openings in doors and covers by using EMI gaskets.
- Include error checking and automatic resets in software.

Keyboards present a special problem. Because of its nature, a keyboard is touched millions of times during its useful life. Spark arresters, special key and keypad designs, and insulating covers are used to minimize ESD effects.

Figure 9 summarizes the various ESD-protection techniques. Proper use of these design techniques will greatly improve total system ESD immunity. These techniques should be implemented at all design levels to produce an optimum design at reasonable cost. (More detailed information on system-level design has been published elsewhere.[19–21])

Product Testing

ESD stressing is done using simulators that are designed to produce the idealized ESD waveforms, as nearly as possible. In the subsections that follow, we discuss ESD-testing methods at the three product levels, and review industry standards.

Devices. Both the HBM and CDM are used for testing microelectronic devices. The device HBM uses a 1500Ω resistor and 100-pF capacitor. A critical issue in HBM-simulator design is to minimize parasitic circuit elements. Early simulators had poor parasitic control[22] and produced unreliable results.[23] More stringent calibration requirements have been incorporated into the standard test methods, and data correlation between simulators has improved.

To test a device, a single pin is zapped while various combinations of the other pins are grounded. The pin combinations fall into these categories:

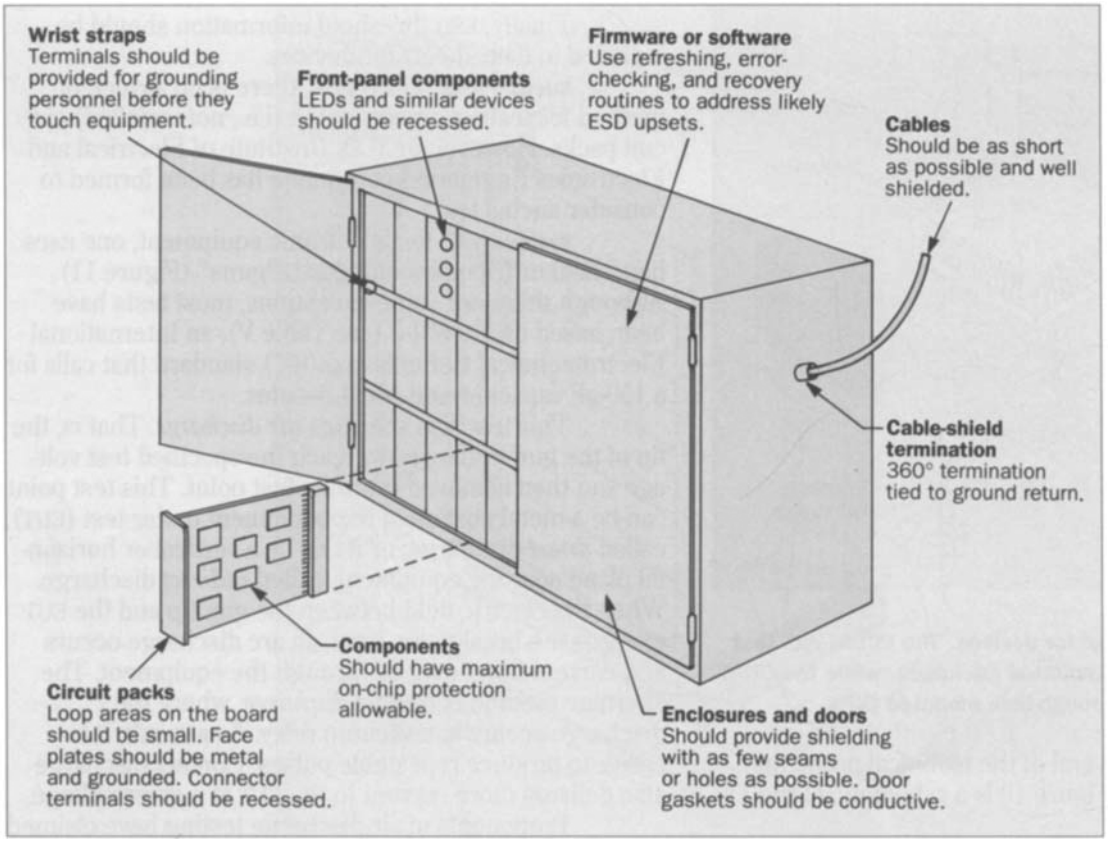


Figure 9. ESD-design considerations involve components, circuit packs, cabling, cabinets, and software.

- Input/output versus power/ground.
- Input/output versus other input/output.
- Power/ground versus other power/ground. This category is a recent addition. It reflects a growing concern about the internal failures that can occur when parasitic transistors are turned on by differential voltages on power and ground buses.[24]

However, considerable controversy still exists over how extensively each category should be explored.

Some companies have also proposed a variation of the HBM in which a dead short replaces the 1500Ω resistor. However, the circuit-parasitics issue with this "machine" model is much more severe, and no industry standard is likely to appear soon.

CDM testing is receiving increased attention. A committee of the EOS/ESD Association is working on a draft test-method standard that should be ready the end of 1990. AT&T has been testing devices using the CDM since 1984. Until recently, this test method was limited primarily to devices in through-hole mounted, dual-in-line packages (DIPs). Now, AT&T has introduced a new CDM method that is based on the principle of static induction.[3,25] This method, which we call the *field-induced CDM* (FCDM), can handle a wide variety of surface-mounted

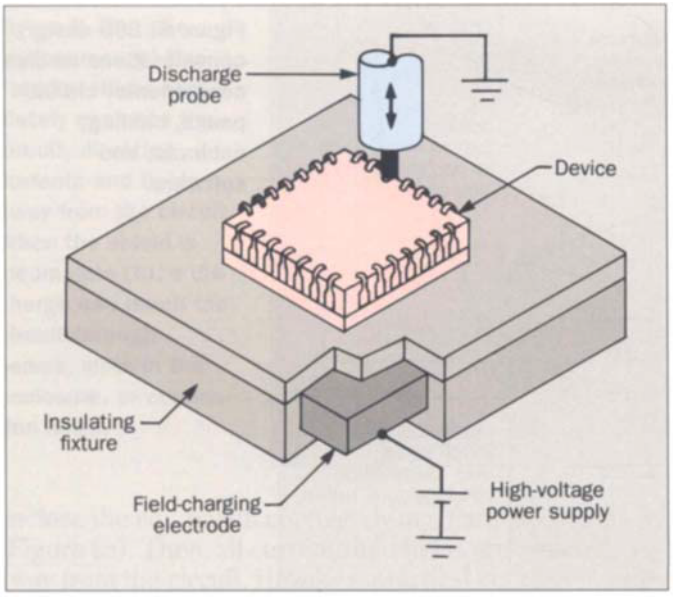


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Figure 10. FCDM simulator for devices. The FCDM can test a wide variety of surface-mounted packages, while the CDM is restricted to testing through-hole mounted DIPs.

packages and solves several of the technical problems with the old approach. Figure 10 is a schematic of the FCDM method.

Some important points to remember about ESD testing of devices are:

- Because ESD sensitivity is extremely dependent on circuit layout, all new codes should be tested.
- Testing should be done as early in the design cycle as possible, so that manufacturing and system-level tradeoffs can be identified.
- HBM sensitivities are independent of package type. But larger packages tend to have lower CDM thresholds (because of the higher capacitance).
- ESD is a high-frequency phenomenon. Therefore, the parasitic effects of sockets or ground returns must be minimized. That is, don't think dc (direct current)!

Finally, ESD threshold information should be included in data sheets for devices.

Circuit Packs. Currently, there is no agreed-on method for testing unterminated (i.e., not installed) circuit packs. However, an IEEE (Institute of Electrical and Electronics Engineers) committee has been formed to consider such a test.

Systems. To test electronic equipment, one uses hand-held or tripod-mounted ESD "guns" (Figure 11). Although there are some exceptions, most tests have been based on IEC 801-2 (see Table V), an International Electrotechnical Commission (IEC) standard that calls for a 150-pF capacitor and 150Ω resistor.

This test also specifies *air discharge*. That is, the tip of the gun is allowed to reach the specified test voltage and then is moved toward a test point. This test point can be a metal portion of the equipment under test (EUT), called *direct* discharge; or it can be a vertical or horizontal plane near the equipment, called *indirect* discharge. When the electric field between the gun tip and the EUT exceeds the breakdown level, an arc discharge occurs and current flows over or through the equipment. The alternate method is *contact discharge*, where the discharge occurs in a vacuum relay. As a result, it is easier to produce repeatable pulses. Contact discharge also delivers more current to the EUT at a given voltage.

Proponents of air-discharge testing have claimed that it is more realistic. However, direct-contact discharge sometimes more closely replicates a person touching a metal portion of the EUT with a metal object, such as a screwdriver, than does the air-discharge test. Further, indirect testing can produce yet another set of different responses. In any of these methods, it is important to adhere to the specified method of grounding the ESD guns, because the ground return can dramatically affect results.

Over the past several years, most telecommunications equipment has been tested using direct-air discharge, and ANSI has adopted air discharge (direct and indirect) in ANSI T1.308, the major standard for central-

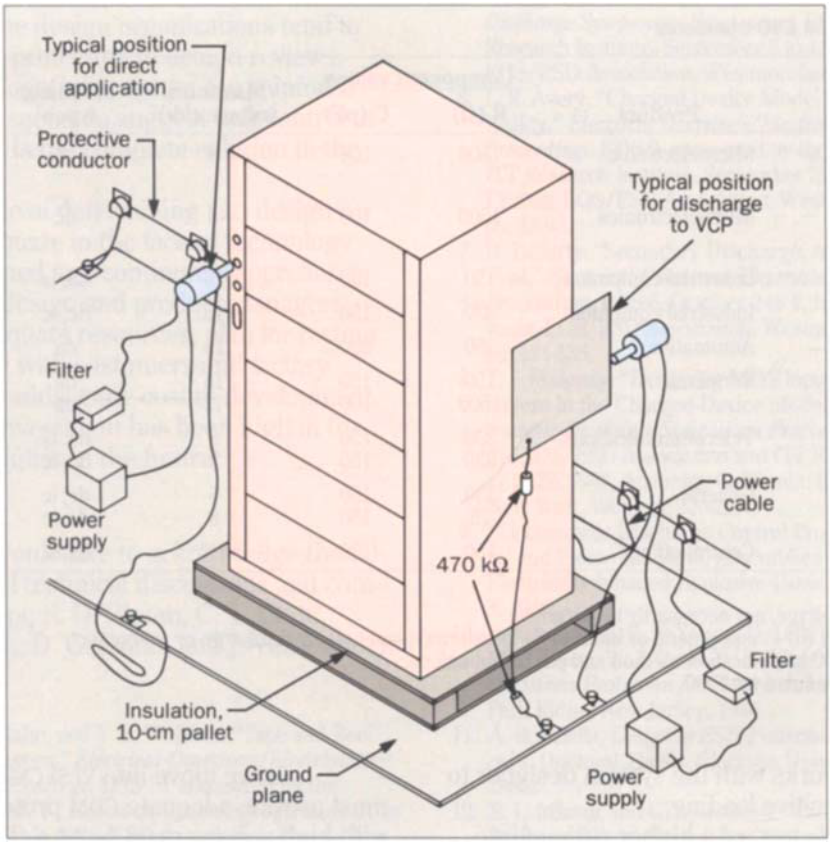

Figure 11. Typical setup for ESD testing of operating equipment (IEC 801-2). An ESD arc discharge occurs as the hand-held (or tripod-mounted) gun approaches the equipment under test. Discharges are made to the equipment, or to a nearby vertical conducting plane (VCP).

office switching equipment. (ANSI is the American National Standards Institute.) However, the IEC 801-2 and CISPR standards are being revised, and it appears that contact discharge (direct and indirect) will be preferred in the future. (CISPR is the International Specification Committee on Radio Interference.) The CISPR standard will be the basis for the ESD requirements adopted by the European market in 1992.

Voltage requirements and failure criteria tend to be product-specific and are negotiated between supplier and customer, although some standards include recommended performance levels.

ESD Design—Dealing with Trends

In the future, the drive for higher speed and performance will continue to push ESD withstand thresholds lower. At the same time, the trend toward high-throughput manufacturing processes will continue to transform assembly factories. High-speed telecommunications equipment will require greater attention to noise reduction, while a competitive marketplace will demand cost reduction wherever possible.

At each of the design levels, techniques are available that can be applied. Even devices that operate at several gigabits per second can tolerate *some* protection,

Table V. Summary of Industrial ESD Standards

Standard or organization	Product	Component values R (Ω)	Component values C (pF)	Maximum voltage (kV)[1]	Discharge types[2]
MIL STD 883, Method 3015.6 (reference 26)	Microelectronics	1500	100	8	dc
EOS/ESD-DS5[3,4] (reference 27)	Microelectronics	1500	100	8	dc
IEC 801-2 (1984)	Industrial equipment	150	150	15	da, ia
IEC 801-2 (1989)[4]	Industrial equipment	330	150	15	dc, ic
SAE	Automotive	250	200	15	da
EIA PN-1361	Terminals	150 1500	150 100	15 15	da da
CISPR (Europe)[4]	Telecommunications	330 330	150 150	8 3	da, ia dc, ic
ANSI C63	General	330 75	150 150	6 6	dc, ic dc, ic
ANSI T1.308[4]	Central office	150	150	15[5]	da, ia

NOTES:
1. Indicates maximum test voltage, not necessarily requirement.
2. Discharge types are: direct (d) to equipment, or indirect (i) to external plane; (a) air discharge or (c) contact.
3. Differs from MIL STD 883C in calibration method and pin combinations.
4. In final stages; release scheduled for 1990.
5. Requirement is 8 kV.

if the device designer works with the system designer to deal with the extra capacitive loading.

While the trends toward a higher scale of integration and high speed present technical challenges, some of the major barriers to producing optimal ESD performance are not technical. The spread in the thresholds for MOS and bipolar devices in Figure 6 is due less to the intrinsic sensitivity of the device, than to the variation in the amount of effort a designer and his or her management give to ESD protection.

Sometimes, the fabrication process may unnecessarily limit a designer. Thus, ESD performance should be considered during *process development*, before the first specific design is completed. Once the process is frozen, the device designer must deal with producing adequate performance.

As we move into VLSI CMOS technologies, we must provide adequate CDM protection to be compatible with high-volume manufacture. This is important to keeping down manufacturing (assembly) costs. The situation is aggravated because the CDM withstand thresholds decrease with increasing package size (capacitance).

In many companies, attention to ESD design tends to occur in bursts every few years. Each burst is usually motivated by some catastrophic event—a major field failure, serious yield losses or lost equipment sales—and may last months or years. But ESD design eventually is reduced to selecting from a few buffers in a design library, or specifying the same cabinets as the previous designer—without regard to changes in technology or manufacturing requirements.

Because ESD failures do not occur every day or,

at least, not visibly, some design organizations tend to give low priority to ESD protection in design reviews. Ironically, a successful control program can reinforce this attitude because it seems to suggest that control of the event in the factory is the complete solution to the problem.

The burst mode of determining ESD design priority will not be adequate in the face of technology trends. A more disciplined and continuous approach to ESD design starts with design and product managers. They must provide adequate resources, plan for testing time, and communicate with customers and factory engineers. This clearly adds some cost to development, but the return on this investment has been high in the past and will be even higher in the future.

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