MANUFACTURING EXECUTION: CIRCUIT PACKS

Robert E. Albano, Cagatay Buyukkoc, Bharat T. Doshi, David X Callaway, David J. Friedman, Terry R. McClure, Laurie A. Schmitt, and John J. Svitak

Robert E. Albano *and* ***David J. Friedman*** *are with AT&T Bell Laboratories at Murray Hill, New Jersey.* ***Cagatay Buyukkoc*** *and* ***Bharat T. Doshi*** *are with AT&T Bell Laboratories at Holmdel, New Jersey.* ***David X Callaway, T. R. McClure,*** *and* ***Laurie A. Schmitt*** *are with AT&T Business Communications Products at the Denver Works.* ***John J. Svitak*** *is with AT&T Bell Laboratories, Princeton, New Jersey. Mr. Albano is a distinguished member of technical staff in the Manufacturing Systems Engineering Department. He works in various AT&T factories to implement just-in-time and total-quality-control manufacturing methods. He has a B.S.E.E. from New Jersey Institute of Technology and an M.B.A. from Rutgers University. He joined AT&T in 1968. Mr. Buyukkoc is a member of technical staff in the Performance Analysis Department. He works on*
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The architecture[1] of the Definity® 75 and 85 telecommunications switching systems is designed to be flexible so that system configurations can be designed to match customers' specific needs. One aspect of this flexibility is achieved through physically standard modules or building blocks (for example, circuit packs), of which there are several hundred. A customer interface engineer can select from these to design a customized PBX for the prospective user. As a result, there is great variability from one customer system to another. At the manufacturing level, this variability is reflected by highly volatile weekly demands for specific circuit pack codes. The high variability of circuit-pack demand, coupled with the high value of circuit packs, makes the efficient manufacture of circuit packs a high priority for competitive PBX manufacturing. This article reviews the circuit-pack manufacturing initiatives that were launched at AT&T's Denver Works to respond to the competitive challenges of the business.

Introduction

At the start of AT&T's manufacturing improvement initiatives in 1985, circuit-pack manufacturing was characterized by high work-in-process (WIP) inventories, long and highly variable assembly and test intervals, unacceptable internal quality levels and, not surprisingly, high cost. In order to continue to be competitive in the PBX business, it was necessary to make major improvements in the circuit-pack manufacturing process. Teams consisting of manufacturing engineers and AT&T Bell Laboratories product developers and manufacturing system engineers were formed. They were given the charge to:

- Improve internal quality.
- Reduce manufacturing intervals and variability.

Panel 1. Acronyms and Abbreviations in This Paper

BOM	bill of materials
DFM	design for manufacturability
DFT	design for testability
DIP	dual-in-line package
EIA	Electronic Industries Association
FTY	first-test yield
IC	integrated circuit
JIT	just in time
MRP	material requirements planning
PBX	private branch exchange
PPM	parts per million defective
SM	surface mount
TQC	total quality control
VAY	value-added yield
WIP	work in process

Quality Improvements

Quality improvements were directed at testing, components and design, and assembly operations.

Testing. In the manufacture of circuit packs, a series of tests is performed. The first is usually in-circuit testing, which uses a "bed of nails" fixture to contact conductors on the back of a circuit pack to check for proper interconnection (no opens or shorts), proper discrete component values, and proper values of certain device parameters. The second is functional testing, which exercises the specific capabilities of circuit packs at operating speed. Finally, the individual circuit packs are assembled into the customer-specified configuration and the functional capabilities of the system are exercised and tested. This last test is known as system testing.

At the start of the improvement project, first-test yields of 55 percent at the in-circuit test and 95 percent in the systems test were the norm. The low first-test yields did not compromise the quality of the product being provided to our customers, but the repair and retesting required to obtain a final test yield of 100 percent was costly.

To support first-test yield improvement and lower the cost of quality, an on-line yield and defect reporting system was put in place for in-circuit testing. Defects were classified into three categories: assembly, testing process, and component. As a result of the data collection and analysis, several symptoms and problems were uncovered. One symptom was that some circuit packs, although identified by the test set to have failed, were being passed by the person conducting the test because, in the tester's judgment based on experience, the test set had falsely indicted the pack. In other words, testing had become an art rather than a science.

Some of the specific actions taken included:

- Standardizing test set maintenance and calibration
- Redesigning interconnection fields between the test set and fixtures and scheduling fixture maintenance
- Verifying that tests were both repeatable and consistent between test sets
- Reviewing designs for testability.

The net effect of these actions was that testing became more accurate and reliable and only circuit packs that had passed tests were allowed to move to the next step. At the Denver Works, this is known as *green light* testing.

Components and Design. Starting with the most common failures, the team collected data on failed components and conducted failure mode analyses. These results were reviewed with the component suppliers. When necessary, handling methods were changed, local or vendor tests were modified, and in some cases components were designed out of the product. The philosophy was to improve component quality without incurring the costs of incoming inspection. Incoming inspection is used only for particular components to support the vendor quality improvement process and to protect the plant from defective components until vendor excellence has been achieved.

To further improve first-test yields, a design for manufacturability/testability (DFM/DFT) checklist was developed by a team of design and production engineers. This checklist covers components, printed wiring boards (physical and layout), DFM audits, and testing (system, functional, and in-circuit). The checklist is a "living document," now in its sixth issue, used to evaluate the manufacturability and testability of new and redesigned circuit packs.

The philosophy that quality should be built-in, *not* inspected-in, resulted in increased yields without increased component inspection costs. A preferred-component database was also developed and implemented. This gave the designers a list from which to select components for changes and for new designs. Component consolidation allowed more effective inventory management and assembly improvements. The DFM/DFT process has helped to decrease the number of component codes supported by 65 percent.

TQC in Assembly Operations. Besides improving test and component quality, it is also necessary to ensure process control. The application of total quality control (TQC) to manufacturing has been outlined by Feigenbaum,[2] who emphasizes:

1. Elimination of operations that do not add value (e.g., inspection and repair operations)
2. Application of statistical quality control and root-cause analysis to permanently eliminate defects
3. Migration of responsibility and authority for process quality to the process operator.

On the basis of these principles, operators were trained to record defects and to check process quality using sampling plans. Accordingly, process checking was eliminated and operators were instructed and trained to check their processes and stop the flow when necessary. In addition, a separate quality assurance organization was disbanded and the circuit-pack assembly shop was made responsible for the quality of its output. To support the shop, quality control software—developed by the AT&T Bell Laboratories Quality Technology Center—was deployed to collect and archive defect data, and shop and engineering personnel were trained to use the data to analyze defects. For the purposes of solving problems, several TQC teams were organized to support continuous improvement in circuit-pack assembly processes similar to those previously organized for equipment assembly.[3] To reinforce shop ownership of process quality, many teams were chaired by the shop supervisor. Successful, and not so successful, aspects of TQC practice are discussed in Appendix A.

Value-added yield. In addition to implementing the traditional techniques outlined above, it was necessary to define new metrics to drive behavior. Traditionally, the measure of how well a manufacturing operation is performing is based on the first-test yield (FTY), that is, the proportion of circuit packs with no defects detected at in-circuit (first) electrical test. This approach, unfortunately, blurs the difference between value-added operations [such as inserting a dual-in-line package (DIP) component into a circuit pack] and non-value-added operations (tasks that do not add value to the product, such as inspection, rework, or touch-up). A manager seeing a first-pass yield of 90 percent has no idea whether this is a product of effective manufacturing or extensive touch-up prior to the first electrical test.

An adjunct to first-test yield is a metric that measures the quality of only the value-added assembly processes. The value-added yield (VAY) uses manufacturing defect levels to calculate the expected process yield. To calculate this statistical measure of process performance, the following assumptions are necessary:

1. All data are collected prior to any rework.
2. All defects are fixed prior to subsequent processing.
3. All defects occur independently, both within a circuit pack and between circuit packs.
4. All defects are consistent with the inspection method (for example, visual inspection assumes no nonvisual defects).

Defect data are often associated with the number of leads or number of components having a defect and are reported in parts per million defective (PPM). We will assume independence of defects and derive a VAY measure based on PPM rates. The expected yield of a circuit pack, based on the binomial distribution, is p^x, where p is the probability of a good component placement and x is the number of component placements on the circuit pack. Since VAY is the yield over all operations,

$$\text{VAY} = \prod_{i=1}^{k} P_i^{n_i}$$

or

$$\text{VAY} = \prod_{i=1}^{k} e^{n_i \ln P_i} = e^{\sum_{i=1}^{k} n_i P_i}$$

Table I. Data for Eight Value-Added Operations

Area	Defect rate (PPM)	Number of operations	Success probability	VAY term (percent)
Tape sequence	1000	200 insertions	.999	81.8
SM paste	300	20 devices	.9997	99.4
SM placement	5000	20 devices	.995	90.5
SM reflow	200	1000 leads	.9998	81.9
DIP insertion	1000	150 insertions	.999	86.1
Axial insertion	800	200 insertions	.9992	85.2
Hand insertion	500	50 insertions	.9995	97.5
Soldering	50	5000 leads	.99995	77.9

where $P_i = 1 - (\text{PPM of area } i)/1{,}000{,}000$ and n_i is the number of inserts in area i.

For example, assume there are eight value-added operations used to manufacture a circuit pack. For each operation, the defect rate, the number of components, and the probability of producing a good component placement are as shown in Table I. VAY is computed as the product of the individual operation probability multiplied by the number of components at each operation.

$$\text{VAY} = \exp\,[200 \ln(.999) + 20 \ln(.9997) + \ldots + 50 \ln(.9995) + 5000 \ln(.99995)] = 34\%$$

The impact of inspected-in quality can be demonstrated by the difference between the VAY and the FTY. If the FTY was 75 percent, the difference between the two yields is 41 percent, attributable to non-value-added inspection and rework. It should also be clear that PPM defect rate is not the only metric to be used for targeting areas for quality improvement. For example, although the defect rate at surface-mount (SM) placement exceeds the defect rate at soldering by two orders of magnitude, SM placement decreases the yield by only 9.5 percent (i.e., 1 – .905), compared with a 22 percent (i.e., 1 – .779) yield loss in the soldering operation. Thus the operation defect rate and the number of components should be considered when selecting an operation for improvement.

Assembly quality results. Activities like those described in the total-quality-control case studies (Appendix A) were repeated many times. Figure 1 shows the results for DIP and axial-lead-component insertion, illustrating the exponential reduction of defects that was typical of the other processes.

These assembly process improvements, coupled with the quality improvements in incoming components and circuit-pack design, increased first-test yields (in-circuit testing) from 55 percent to greater than 90 percent. Non-value-added operations in circuit-pack assembly (process checking, inspection, touch-up, repair, and quality assurance inspection) were reduced from 40 percent to 10 percent of assembly shop operations. Moreover, the non-value-added operations are now primarily high-speed automatic inspection processes that promptly feed back quality information to assembly and support continuous improvement.

Reducing Intervals and Variability

Concurrently with the complementary quality improvements, a program was conducted to reduce manufacturing intervals and variability by reengineering the flow of material.[4] At the start of this program, the average circuit-pack manufacturing interval was over 2 weeks, with a distribution ranging from 1 day to greater

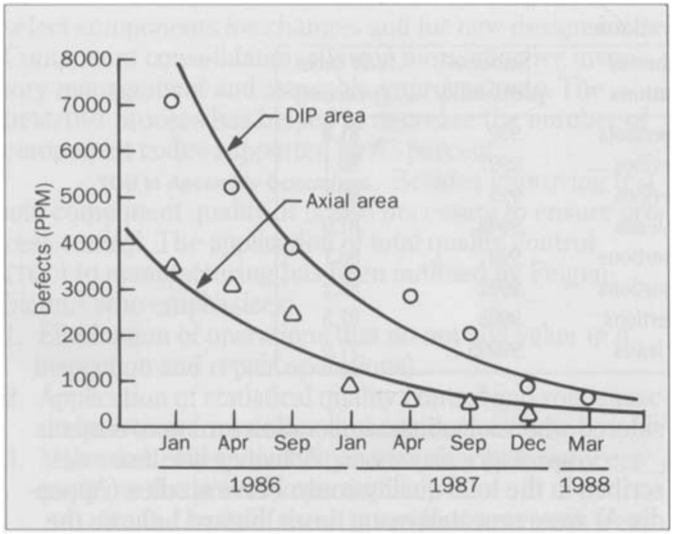


Figure 1. The incidence of defects decreased steadily over several months' time as a result of total-quality-control team efforts. The data here for assembly of DIP and axial-lead components are typical of that for other processes.

than 50 days. The long intervals were a result of unwanted material being pushed from the storeroom and to a lack of disciplined material flow procedures once the material was delivered to the shop floor. The strategies used to resolve these issues will now be described.

Pull from the Storeroom. The material requirements planning (MRP) system generates a pick list, a list that instructs storeroom personnel what to pick from the storeroom and deliver to the shop floor, so that the necessary material is available for manufacturing products to meet customer orders. Unfortunately, the pick lists were generated weekly and did not necessarily reflect the daily needs of the shop. Furthermore, the pick list items, or "picks," were pushed onto the shop floor regardless of the shop floor's ability to accommodate the material.

The net effect was that the storeroom and the shop were not working together and were often working on items that were not of high priority. When a high priority item did arise (a daily occurrence), the storeroom and the shop "dropped everything" and worked on the "hot" item. The end result was longer average intervals and greater variability.

To resolve this conflict, the storeroom agreed to hold the picks until they were requested by the shop. This "pull" strategy allows the shop to focus on assembling circuit packs that are required in downstream operations without the distraction of managing extraneous "pushed" material. A simple electronic pull system was designed in which the shop and storeroom had linked, identical terminal screens. When a pick is available, the storeroom operator enters the pick number, description, and quantity, and the entry is time- and date-stamped and displayed. When the shop is ready to start assembling additional circuit packs, it requests an available pick by positioning the cursor and striking an execution key. The storeroom delivers the pick, and with a single key stroke on the shop terminal, denotes the pick as delivered. The pick record is time- and date-stamped and removed from the screens. The time/date stamps track problems and provide information such as pick staging interval, picks staged daily, and the storeroom delivery interval.

Material Flow. Though holding material in the storeroom until it was requested helped, there was still considerable excess material on the shop floor. Further improvements in material flow and reductions in manufacturing lot sizes (number of circuit packs of the same code processed in a group) would require major changes in the way the shop managed material flow.

The machine assembly area was chosen because it accounted for a large portion of the total work in process and was a major source of variability. Specialized machines are used to insert different types of components, stencil solder paste, place different types of components for surface mounting, reflow-solder, and automatically inspect for the presence of inserted leads. Because some circuit-pack codes might require many

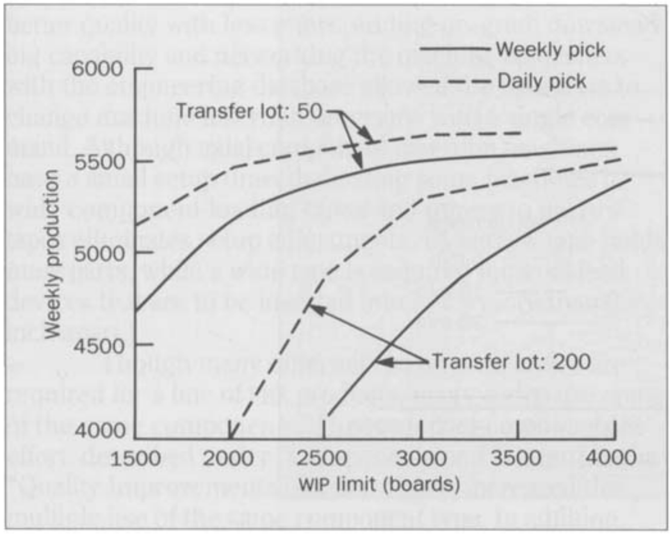


Figure 2. Production is substantially higher with daily instead of weekly picks, and with smaller transfer lots (50 versus 200), particularly at lower WIP limits. Data are for a setup time of 15 minutes for each operation.

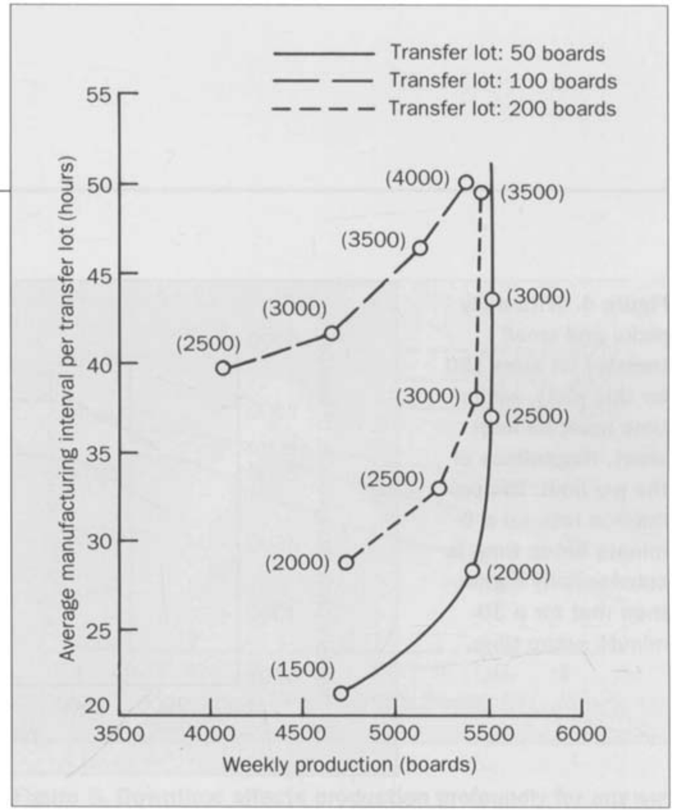


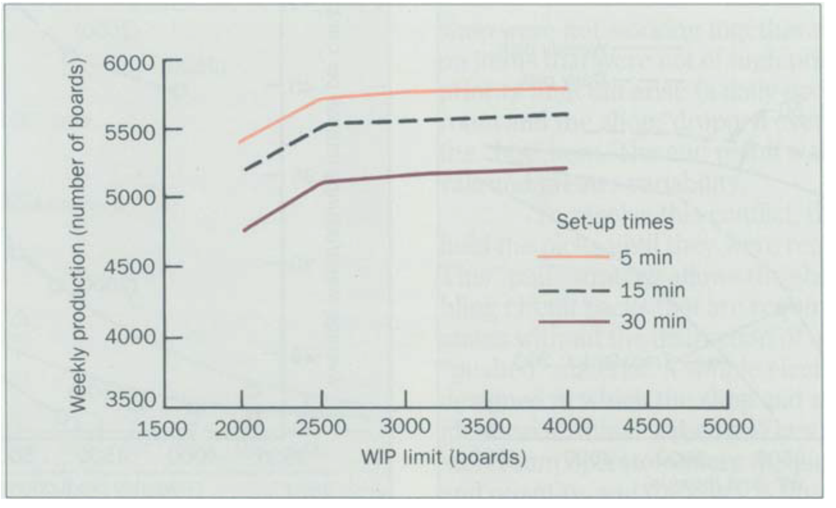
Figure 3. Effect of transfer lot size: manufacturing interval decreases and production increases as the transfer lot size is made smaller. The numbers in parentheses represent WIP limits. The setup time is 15 minutes per operation.

resistors (inserted by a variable-center-distance machine for axial-lead components) while others require many large surface-mounted devices (requiring several special surface-mount machines), the processing times through the machines are quite different. To utilize these facilities efficiently, several codes of circuit packs are routed through the specialized machines simultaneously. Tradeoffs between complex factors must be quantitatively understood to plan for a major improvement.

One of the factors is the number of circuit packs of the same code that are available for processing together (manufacturing lot size). In practice, the maximum manufacturing lot size was whatever the storeroom delivered (up to six lots of 200 circuit packs each). Such large lots cause very uneven demand on the processing machines because different codes have widely different processing times. On the other hand, small lots mean that machines must be frequently stopped and prepared for processing a different code (set up).

Another factor influencing interval is the transfer lot size (number of circuit packs moved from operation to operation). Typically, the whole manufacturing lot (200 or more circuit packs) would go through one operation, wait for a material handler to move it to the next operation, go through another operation, wait again, and so on. Thus, the manufacturing interval was at least 200 times the actual processing (butt-to-butt) time for one circuit pack. Moving circuit packs in smaller quantities between operations (smaller transfer lot sizes) would tend to reduce the manufacturing interval. However, this breakup of a pick within the line could separate the transfer lots for the same code, causing additional setups. A quantitative understanding of the tradeoffs between the transfer lot size, manufacturing lot size, and

Figure 4. With daily picks and small transfer lot sizes (50 for this plot), setup time must be kept short. Regardless of the WIP limit, the production rate for a 5-minute setup time is substantially higher than that for a 30-minute setup time.



setup time was needed.

And finally, the total number of circuit packs in process (work in process, or WIP) needed to be reduced to shorten the average interval according to Little's law.[5] However, a large number of circuit packs in process provides flexibility so that a disruption (such as machine downtime) or long processing times at one facility do not "starve" downstream operations—that is, idle them because of unavailable work.

The manufacturing improvement team analyzed the machine assembly area by constructing a computer model that simulates the operation of the facilities. The simulation model accommodates any number of codes, code-dependent manufacturing, and transfer lot sizes, as well as code-dependent routing. Periods when facilities are unavailable, either because of a breakdown or because they are being set up for a new code, are included.

A small sample of simulation results is presented in Figures 2, 3, 4, and 5 for a strategy of limiting overall WIP. Figure 2 shows the results for a 15-minute setup time at each operation. The advantages of daily picks and smaller transfer lots are quite clear. Transfer lots of about 50 and a WIP limit of about 2000 circuit packs would be ideal. As shown in Figure 3, increasing the WIP limit beyond 2000 does not add to the production rate but does increase the manufacturing interval considerably. It is clear from Figure 4 that setup times, which were 15 to 30 minutes at most operations, had to be reduced to 5 to 10 minutes to maintain a high production rate with daily picks, small transfer lots, and small WIP limits. Finally, Figure 5 shows that the duration of downtime, if any, had to be maintained under 1 to 2 hours to manage a high production rate with small interval and inventory.

With these parameters, the simulation study predicted that the time for circuit packs to go through the machine assembly processes would drop to about 30 hours (about 2 days of two-shift production) at a sustained production rate of over 5500 circuit packs per week. This is less than one-fifth the interval measured in the tracking study. The methods used to reduce setup times and implement control of total WIP to realize this interval reduction will be described next.

Setup Time Reduction. Some generic changes were used on all assembly machines to reduce setup times. Dedicating a small set of circuit packs to one machine, thus one operator, gave more ownership and resulted in better quality with less effort. Adding program downloading capability and networking the machine controllers with the engineering database allowed the operators to change machine insertion programs with a single command. Although axial-component insertion machines have a small setup time, dedicating some machines to wide component-loading tapes and others to narrow tapes eliminates setup adjustments. (A narrow tape holds most parts, while a wide tape is required for axial-lead devices that are to be inserted into holes more than 0.8 inch apart.)

Though many different circuit-pack codes are required for a line of PBX products, many codes use some of the same components. The preferred-component effort, described under "Components and Design" in the "Quality Improvements" section above, increased the multiple use of the same component type. In addition, there are many components that have different electrical properties, but identical mechanical properties (size, shape, number of leads, etc.). The use of the same components and of mechanically identical components in multiple circuit-pack codes provides an opportunity to reduce setup times drastically. This setup reduction opportunity matched the critical need for improvement in tape sequencing and in DIP insertion. The use of dedication to reduce setup times is schematically illustrated in Figure 6.

Background: Tape sequencer/DIP dedication. The tape-sequencing operation produces sequenced reel tapes, i.e., axial-lead components taped to two strips in a specific sequence, to be used by axial-component (variable-center-distance) insertion machines in the assembly of circuit packs. Each time a different sequence is made on a tape-sequencing machine, a time-consuming change of up to 60 different reeled components is required. Similarly, DIP machines insert integrated circuits (ICs) into circuit packs, and each circuit pack requires a variety of ICs that must be loaded on the machines before the production run. DIP machines select components from up to 65 different tubes that are loaded into machine slots.

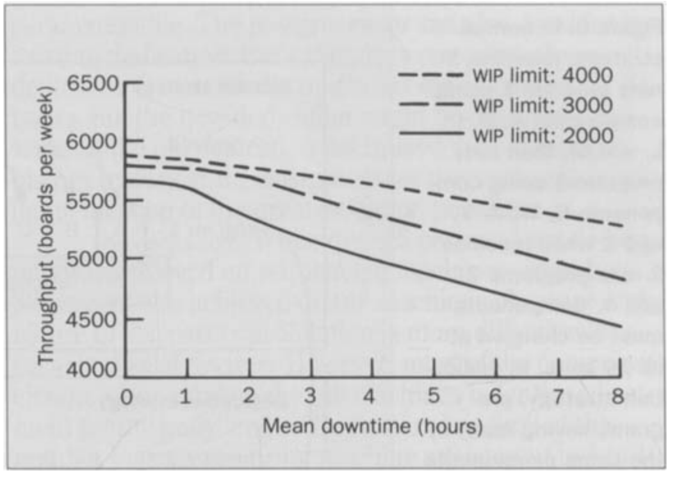


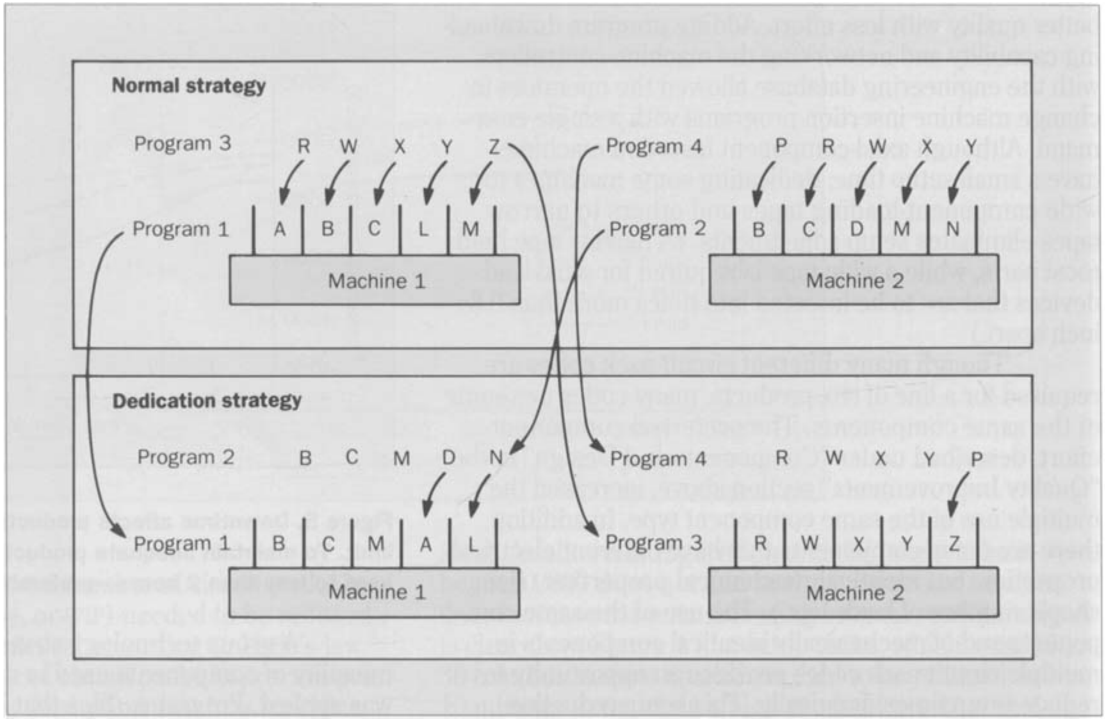
Figure 5. Downtime affects production profoundly for any WIP limit. To maintain adequate production, downtime must be kept to less than 2 hours—preferably less than 1.

A group technology strategy, based on the commonality of components used in different circuit packs, was applied. Programs (files that include the machine instructions and identifications of each component) are grouped into families according to the number of common components, machines are dedicated to the families, and the corresponding components are dedicated to feeder slots on a machine.

Dedicating components on a machine reduces setup time by reducing the number of component changes and adjustments. Components are assigned dedicated positions according to the number of times the component must be loaded and unloaded per week. Remaining positions are for the few components that must be changed. An important operational criterion is level-loading the machines. Near optimal dedication may be achieved by loading some machines to 100 percent and a few machines to only 50 percent of capacity, but this is not a practical strategy for shop operation.

Hard-dedicated slots are slots that dispense only

Figure 6. In normal strategy, machine 1 runs program 1 using components A, B, C, L, and M, then runs program 3 using components R, W, X, Y, and Z while machine 2 runs programs 2 and 4. Components must be changed at all 10 slots. In dedication strategy, programs having many of the same components (families) are assigned to the same machine. Common components are given assigned positions (slots), so many component changes are avoided.



one component. Length-dedicated slots (for DIPs) dispense more than one component, but all of the same length. Undedicated slots require machine adjustment for DIPs and component unloading and loading for DIPs and tape sequences.

Software supporting slot dedication fits into three general categories: providing input data, determining the slot assignments (that is, the dedication), and implementing the dedication. Without accurate and complete input data, dedication is not feasible. The dedication software uses heuristic techniques and operational constraints and minimizes computer run time in order to provide a usable tool. Implementation must be fast, must be accurate, and must use feasible engineering resources. Using dedication to reduce setups requires an integrated set of all three elements.

The input data include current machine instruction programs with the associated weekly load and component information. In general, two files are required: weekly load and a component "grocery" list. Part of the information resides in master-scheduling and bill-of-material databases and part in machine instruction directories.

Sequencer reel slot dedication and DIP tube slot dedication are similar: first, partition machine insertion programs into feasible subsets ("families"); then, adjust the families by shuffling membership according to several constraints and goals. The goal is to reduce setups by assigning as many components as possible to fixed slots (*hard dedication*) and to provide level-loaded families. There is a feasibility constraint for hard dedication—a part cannot be hard-dedicated if doing so would mean that some sequence in the family could not be built because too few undedicated slots remain.

For example, 250 sequences might have over 800 different components, with an impractical number of ways 250 sequences could be divided into 8 families. Given the large numbers involved, an optimizing algorithm for dedication is not practical from a run-time perspective. Accordingly, both types of dedication use heuristics to determine the initial families, shuffle the families to minimize setups, and decide which parts to dedicate. A dedication is obtained by repeatedly running the dedication software tools while changing the parameters for each run until there is little improvement with further runs. The output files for each family provide information on slot assignments, programs assigned to that family, and, for DIP machines, some information about the hardware configuration of the machines. The parameters include hardware configuration, the number of machines available, the required number of families, and the lot size to be used in the particular area. Parameters are set from experience and trial and error, and engineering judgment is used to determine the effectiveness of a dedication.

Tape sequencer dedication. Tape sequencer dedication uses a main program and a postprocessor. After providing the main program with the number of families to be considered, it "seeds" each family with some sequences that are sufficiently dissimilar and high in volume. The main program then populates the families with the remaining sequences. After filling all the families, it allocates the available machines to families, making adjustments if necessary to avoid exceeding machine capacities. The main program then remakes the families to either minimize setups or to maximize the number of component overlaps. After a few iterations or after improvement ceases, the main program balances the loads across the families to a user-specified tolerance and assigns "virtual" machine slots to each component of each family. The virtual machine slots are mapped to actual machine slots by the postprocessor according to operational requirements defined in a user input parameters file. The postprocessor can also consider the existing dedication. For example, a complete change of dedication for ten 80-slot machines would take about 27 hours, but the new dedication might be essentially the same as the old dedication but moved over one slot. A history feature in the postprocessor preserves the existing dedication to the greatest extent possible.

DIP dedication. While over 75 percent hard dedication was achieved on sequencing machines, only about 30 percent was achieved on DIP machines. Because of the nature of ICs, part consolidation is more difficult with DIPs than axial devices. However, most of the component change setup time on the DIP machines is for the adjustment for DIP body length. Dedication has limited the number of parts requiring machine adjustment to 5 to 10 percent of all parts, and these are typically for infrequently built circuit packs.

The basic goals in tape sequencer and DIP dedication problems are similar; however, the details and the algorithms differ significantly. Important differences are the way the initial families are created and the way the members are shuffled. In DIP dedication, the initial families are created to equalize setup times. After initial families have been determined, shuffling is done to minimize setups, then more shuffling is done to level-load families. A second dedication level minimizes adjustments to accommodate different DIP lengths. To dedicate the parts in a family, the number of hard-dedicated components is maximized, then the remaining components are assigned either to length-dedicated slots or to slots that may require adjustment (undedicated slots). The postprocessor assigns the dedicated components to machine positions according to user criteria, e.g., hard-dedicated parts might be placed near the center of the machine to minimize shuttle travel.

Implementation. Implementing a dedication involves three main activities:

1. Changing the machine insertion program database
2. Installing the new programs
3. Printing and distributing shop documentation.

Insertion and sequencer machine instructions are computer-generated to reflect new slot assignments, since several hundred insertion programs may be involved.

For sequencers, computer programs generate setup sheets giving the new slot assignments for each component (one sheet for each different sequence), generate a new verifier test program for each sequence using the new slot assignments, generate machine instruction programs, and batch-install the instructions. A single UNIX system shell program, executed once on each family, performs all these actions. (UNIX is a registered trademark of UNIX System Laboratories, Inc.) The hard-copy setup information for each family used by the shop is generated by a document-printing UNIX system shell executed once for each family.

After DIP dedication, all insertion programs are altered to reflect the new slot assignments by one call to a C language program, and new setup information for each program may be produced at the same time. Setup sheets, giving the hard-dedicated components, the lengths to set the machine escapements (for length-dedicated components), and the machine configuration, are generated. A collated set of documents for use by the shop is made by executing a single UNIX system shell once for each family. In the past, obtaining a dedication took weeks of manual effort, and implementing one was a laborious process of altering hundreds of files, one at a time. Now a trial dedication can be obtained in less than an hour for sequencers and less than 10 minutes for DIPs. Once a dedication is chosen, the changes for more than 250 programs can be implemented and the documentation batch-printed, all in less than 15 minutes.

In addition to dedicating parts feeding slots, operational improvements were implemented to reduce DIP insertion disruptions. Presentation carts hold additional component tubes for replenishment and for the next code that will be processed. Tubes are positioned and labeled in the cart just as they will be used in the DIP insertion machine; this is done for operator convenience and to minimize the chance of errors.

Slot and fixture maintenance was also reduced. In the past, when a slot broke, the operator reassigned the component to a new slot. This postpones the problem rather than fixes it, which is unacceptable with dedication, so new procedures allow no reassignment and require immediate response to slot problems. Dedicated fixtures reduce the need for program offset changes, and a software feature called *board error correction* automatically makes minor offset adjustments; combined, these nearly eliminate manual offset setup.

Setup reduction benefits. The dedication strategy has significantly reduced setup times. The average time to prepare a tape sequencer for processing a new code has been reduced from 1½ hours to 15 minutes. Daily-sized lots are assembled with 20 percent fewer machines than would have been required. Before dedication, a material handler pulled component reels (averaging 20, but up to 60) from storage racks onto carts for the machine operators. Now the machine operator pulls the average of three reels required for setup, and no material handler is necessary. The few necessary reel changes are accomplished with far fewer errors and with less chance of handling damage.

The average time to set up a DIP machine for processing a different circuit-pack code has been reduced from 45 minutes to 5 minutes. DIP dedication has reduced the number of components loaded/unloaded for setup by 30 percent and reduced the number of length change adjustments by over 90 percent. These operational simplifications contributed to the exponential reduction of insertion defects shown in Figure 1.

Limiting total work in process. The final element in re-engineering material flow in the circuit-pack machine assembly area was to limit the total number of packs being processed. The simulation model predicted that the machine assembly area could have less than one-fifth the previous number of circuit packs in process and still not have appreciable starvation because of unavailable work.

A simple mechanism was used to limit the total work in process in the circuit-pack assembly area. A limited number of carts, each holding a maximum of 40 boards (the number moved to the next operation or the transfer lot size), were introduced. This is a variation of normal kanban processes using carts[6] in that the carts are not pull signals for particular codes. Each cart has a card that identifies its present contents, giving the circuit-pack code, quantity, process routing, and space for operator sign-off. Material flow and total work-in-process control was accomplished by asking the shop to:

1. Request material from the storeroom only when sufficient empty carts are available.
2. Keep all circuit packs on the cart unless they are actually being worked on.
3. Move the cart to an area visible to the next process when all its boards have completed a process.
4. Not "split" material on a cart; i.e., if there are repairs to be made on a circuit pack, return the whole cart to the responsible operator.

Empty carts are made available only when circuit packs that started in that cart have been completed successfully and are loaded onto the progressive assembly line for final in-line assembly. This simple mechanism forces the machine assembly area to limit the amount of material that it is working on and has to manage. It makes the shop personnel sensitive to disruptions, because extended or frequent disruptions result in carts of material stagnating, thus limiting the number of carts that are available for serving other processes and for starting new material into the shop. An empty cart becomes a precious commodity that everyone in the shop values.

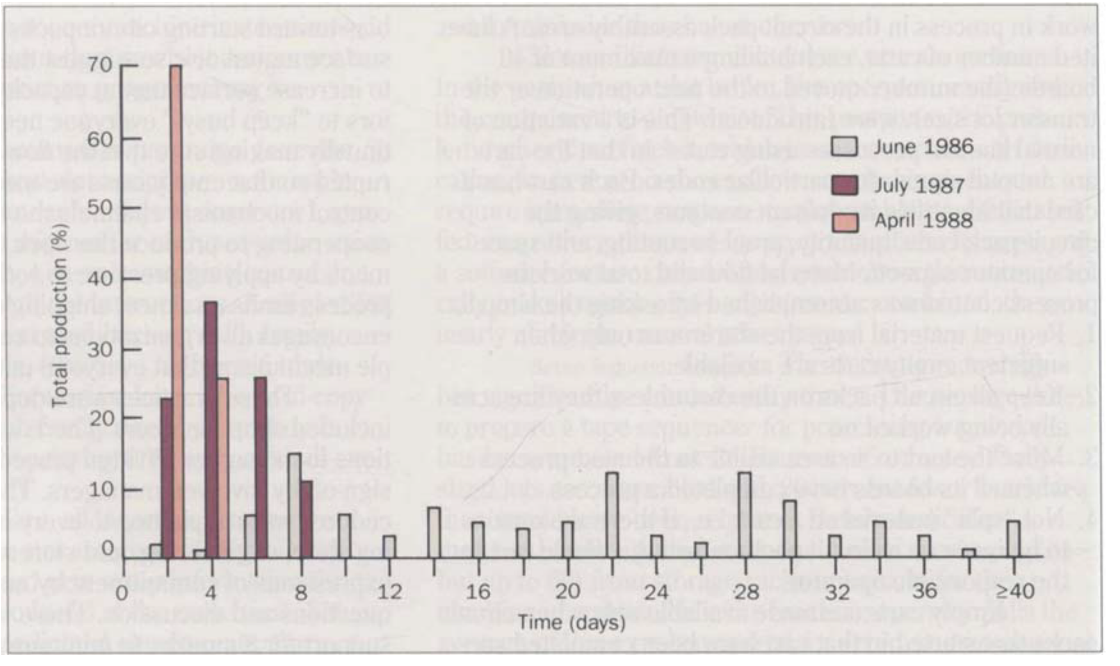
The shop decides what work it will dispatch, how it will manage its buffers, and how it will manage its resources. The reduced number of circuit packs in the shop simplifies the dispatching problem. For example, reduced inventory level allows the on-floor scheduler (layout operator and material handler) to see that most circuit packs present on the floor might require extensive surface mount. The scheduler would then have a bias toward starting circuit packs that require little or no surface mount or else suggest that operators be shifted to increase surface-mount capacity. In order for operators to "keep busy," everyone needs to cooperate, continually making sure that the flow of material is not disrupted so that empty carts are made available. The cart control mechanism channels the desire to keep busy into cooperating to produce the work that is needed. Management, by applying pressure to *both* honor the work-in-process limits *and* meet shipping and quality standards, encourages all organizations to cooperate by using simple mechanisms that everyone understands.

These practices were deployed by a team that included shop members. There were one-on-one explanations to managers. Written procedures were prepared for sign-off by involved managers. The strategy and procedures were explained to every involved person including shop, engineering, and storeroom people, with public expressions of commitment by managers followed by questions and discussion. There was special engineering support for 3 months (a minimum of an hour of checking with shop operations, answering questions, and resolving problems, for all shifts every day).

Progressive hand assembly. The final circuit-pack assembly processes—hand insertion of components that cannot be machine-inserted, wave soldering, solder inspection and touch-up (if needed), and attachment of mechanical parts such as faceplates—are accomplished on a progressive assembly line. Circuit packs are conveyed, one after the other, through up to 30 individual operations. Before setup reduction efforts in 1986, 15 to 30 minutes was required to prepare the progressive line for processing a different circuit-pack code. Thus, the progressive assembly lines processed large numbers of the same code of circuit pack to avoid idling the line operators and equipment.

The concepts of preparing for changeovers off-line, or externally, and of simplifying the whole change-over process[7] were used to reduce setups and disruptions of the progressive assembly lines. Preparing

Figure 7. Over approximately a 1-year period, from June 1986 to July 1987, the average assembly time for circuit packs was cut from more than 2 weeks to about 4 days. By April 1988, 70 percent of total circuit-pack assembly was done in just 1 day.



components was moved off-line and enhanced to provide only accurately trimmed and formed components. This not only eliminated further forming by the assembly operators, but also reduced postsolder trimming and the risk of lead clippings remaining on circuit packs. The external component preparation operation loads individual trays with exactly the right components required by each of the operators to process the next circuit-pack code. These component trays are loaded into presentation carts by a material handler while operators are actively processing other circuit-pack codes. The parts presentation carts have rotating shelves (similar to those in jewelry display cases) that position the preloaded component trays for the next circuit-pack code in seconds.

Three activities further improved assembly and reduced the number of components requiring lead clipping and forming:

- Engineers worked with component vendors to change the lead lengths and lead forms.
- Designs were changed to use new components and/or component "footprints"—the sizes and shapes of the areas occupied by components on a circuit board. Now, only 30 percent of the components preloaded into the trays require trimming and forming, as compared with 90 percent a few years ago.
- Feeding mechanisms for commercially available automatic insertion machines were modified so that parts that were formerly inserted by hand are now inserted automatically at lower cost and with lower assembly defect rates.

Pictorial representations of the circuit packs are used as assembly aids. Previously, engineers marked circuit pack assembly drawings to indicate each assembler's parts and, to aid process checking, those of the previous assembler. A system generates these pictures from the common design file, and they are easily updated to reflect any changes. The assembly aids are displayed on color monitors and are changed by the operator as needed for a new code, without any setup delay. This system not only eliminates flipping through paper aids to find information for the next code, but also provides the latest version with much less engineering effort.

With the setup improvements discussed so far, circuit-pack codes of the same width can be changed over quickly. The operators switch to the new code during their normal circuit-pack processing time, so that the new code follows right behind the old code.

When switching to packs having a different width, an operator used to place a circuit pack into the feeding mechanism and make manual adjustments. Now, the operator adjusts the feeding mechanism by digitally setting the predetermined width; trial-and-error manual width adjustment is unnecessary. Width can now be adjusted as soon as the line is clear.

Material flow: Results. By July 1987, circuit packs were being assembled in an average of 4 days, compared to over 2 weeks a year earlier, as shown in Figure 7. Further, assembly interval was more predictable, with every board completed within 10 days of starting compared to over 2 months during the tracking study. These results were achieved not by making processes work faster, but by reducing waiting time and disruptions. Equipment maintenance programs[3] and the quality programs reduced disruptions, product repair, and retesting. Shorter setup times reduced idle time and allowed processing smaller lots. Implementation of pull from the storeroom, smaller lots, and a limit to the total number of circuit boards being processed drastically cut the time that boards were waiting to be processed. The more than threefold reduction in interval (and in circuit pack in-process inventory) was accomplished without new processing equipment or even rearrangement of existing equipment. Sophisticated and complex technology was not used to manage complex operations; instead technology was selectively applied to *simplify* shop operations (by reducing setup times and identifying disruptions, for example). The reduced level and the visibility of the work in process (the "WIP control" carts have bright color-coded bars to identify the owning shop) allowed each shop to manage flow through centralized surface-mount facilities in other shops as well as through its own facilities.

Summary and Epilogue

Figure 7 shows the distribution of intervals in April 1988 with reconfigured circuit-pack assembly processes. Overall, there has been a greater than fivefold improvement in material velocity as a result of the quality and interval initiatives. Furthermore, in comparison with a few years ago, the same number of circuit packs are assembled and tested in half the floor space—and they have higher yields and far fewer defects.

Even more important, improvements continue to be made even after the "official" end of the previously discussed initiatives. For proponents of just-in-time (JIT) supply methods, this is not surprising, since once the JIT process is started, there are synergies that facilitate continuing improvement. Reductions in defects and disruptions allow shorter intervals and result in less inventory. The shorter intervals allow quality problems to be quickly brought back to the responsible operator and corrected before more defects can be created. Reduced inventory makes the processes visible, and further improvement opportunities become apparent.

Some of the postinitiative improvements were:

1. Reallocating the central surface-mount assembly facilities to provide each shop with all the capabilities needed to process its products..
2. Consolidating facilities in a U shape to enhance teamwork and material flow.
3. Placing many facilities in-line.
4. Introducing a finite buffer between solder paste printing and placement of surface-mount devices. This improved velocity and ensured consistent

solder paste properties during placement.

Circuit-pack test has also seen improvement. Previously, large lots of circuit packs were pushed to the circuit-pack test area. An informal "hot list" was used to pull pack codes that were needed to complete systems from the resulting buffer. As the assembly shops began shipping smaller batches (lots) of circuit packs that matched daily requirements for customer systems, the number of circuit packs waiting to be tested dropped by a factor of more than 3. The drop in component and assembly defects reduced the need for repair and retesting. An extremely complex, consolidated testing operation became uncluttered and understandable and, therefore, easier to manage and more cost-effective.

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Biographies (continued)

modeling and analysis of computer and communication networks and queuing systems and on combinatorial optimization problems. He received B.S. and M.S. degrees in electrical engineering from Orta Dogu Teknik Üniversitesi and a Ph.D. in electrical engineering/computer science from the University of California, Berkeley. He joined AT&T in 1984. Mr. Doshi is a supervisor in the Performance Analysis Department. He and his group develop general methods and tools for performance analysis and analyze and improve the performance of computer, communication, and manufacturing systems. He received a B.Tech. in mechanical engineering from the University of Bombay and an M.S. and a Ph.D. in operations research from Cornell University. He joined AT&T in 1979. Mr. Callaway is an engineer in Information Systems Development. He develops software for manufacturing, including placement of circuit-pack parts. He has a B.S. in mechanical engineering from Colorado State University. He joined AT&T in 1985. Mr. Friedman is a member of technical staff working on applications of statistical process control in manufacturing, especially in integrated circuit manufacture. He joined AT&T in 1986 with a B.E.S. in engineering science from the Johns Hopkins University and an M.S. in operations research and Ph.D. in industrial and systems engineering, both from Georgia Institute of Technology. Mr. McClure is an occupational engineer in the Business Communications Systems Manufacturing Department. He is responsible for coordination of the Definity® telecommunications system circuit-pack product engineering team and for representing the department at Definity system commonality meetings and on the Definity System Field Change Review Committee. He received a B.A. in political science from the University of Wyoming and a B.S. in mechanical engineering from Colorado State University. He joined AT&T in 1985. Ms. Schmitt is a planning engineer in the Process Engineering Department. She works on development and implementation of factory just-in-time concepts and material flow analyses. She has a B.S.I.E. from Iowa State University. She joined AT&T in 1986. Mr. Svitak is a supervisor in the Manufacturing Systems Engineering Department. His work involves improving manufacturing performance by on-site application of systems engineering, just-in-time, and total-quality-control principles. He has a B.S. in mechanical engineering from the University of Maryland, an M.S. in engineering mechanics from New York University, and a Ph.D. in engineering materials from the University of Maryland. He joined AT&T in 1961.

Appendix A: Total-Quality-Control Examples

Three examples will be cited in this section. The first two illustrate TQC team successes in resolving problems. The final example illustrates a problem that is beyond the scope of a TQC team's authority.

Example 1: Progressive Assembly Line. Pareto analysis of defect data over a 3-month period showed that a single component represented 15 percent of all assembly defects. The component, a crystal, was not checked during in-circuit testing and therefore did not surface as a problem in first-pass yield data. The shop supervisor assigned the crystal problem to the product engineer. The layout operator suggested that the component was difficult to insert by hand because other components obscured the holes into which the crystal was to be placed. Another team member speculated that the height of the component might be causing it to fall over. To solve the problem, the product engineer rebalanced the assembly line so that the crystal was inserted earlier in the assembly sequence. In addition, tape was applied to the crystal to hold it vertical. These changes were implemented within 1 week, and when the team followed up 2 months later, the problem had disappeared.

The team then turned its attention to the next most serious problem, high-profile two-pin capacitors. The product engineer determined that their location and height made them susceptible to being brushed by workers inserting other parts. The line was again rebalanced to delay the insertion of these capacitors, reducing their defect rate by 61 percent.

Example 2: Axial Insertion Machine. An axial-lead capacitor occasionally cracked during insertion. The team theorized that the problem might be caused by the capacitor length. The assigned process engineer qualified a new capacitor vendor in 6 weeks. With the cooperation of the shop, both vendors' capacitors were evaluated.

The root cause of the cracking was found to be a missing component body length specification; the standard part exceeded the insertion machine limit for body length. Since the standard component could not be modified, the new vendor became the supplier of choice.

Continuing process improvements, the layout operator observed that the speed of the axial insertion (variable-center-distance) machine appeared to be too fast for these capacitors. Working with process engineering, the maintenance mechanic (a TQC team member) adjusted the speed of the axial machines, and the defect rate was reduced further. The action item was closed after 13 months, but its impact was a 20-fold reduction in the defect level for cracked capacitors.

Example 3: Solder Accumulation. A persistent problem was the accumulation of solder on insertion machine tooling. Analysis showed that the solder coatings on the tooling had a high lead content. It was clear that the problem could be eliminated by reducing the solder's lead content. However, this would require adoption of new solder composition specifications by the Electronic Industries Association (EIA). Eliminating this problem was therefore outside the responsibility, authority, and capability of the TQC team, and it was referred to the AT&T representative on the EIA committee.

Analysis. Common threads run through these three examples:

1. *Timely Problem Identification.* In all three studies, the problems were presented to the team in a timely fashion.
2. *Cooperation.* In the first example (the crystal), the product engineer had to change the division of tasks on the progressive assembly line and the shop had to add an additional taping step. In the second, a vendor cooperated to resolve the capacitor problem. In the third (solder accumulation), there was a need for industry-wide cooperation.
3. *Leadership.* The shop supervisor was recognized by all members of the team as having the authority to assign action items and due dates. The leader has an obligation to control the tone and the direction of the meeting and must be the final arbiter on issues of ownership and action item assignment. When the managers of the team members support the leader,

engineers, and shop personnel involved in the TQC team, the team is extremely effective.

4. *Progress.* Progress must be made continually, although this does not always mean resolving issues quickly. Aggressive attempts to solve certain problems quickly, such as the crystal problem, need to be matched by persistent efforts to resolve certain other problems, such as the capacitor problem. Even the solder accumulation problem was promptly referred to a more appropriate group.
5. *Follow-up.* In all cases, there is follow-up until there is clear evidence that the problem has been resolved; otherwise, the item is left open.

(Manuscript received April 23, 1990)