REACHING THE LIMITS IN SILICON PROCESSING

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The trend in silicon device fabrication of employing increasing numbers of more complex processes to produce materials systems with narrower tolerances of performance has produced encounters with some fundamental limits of materials processing. This paper examines the role of materials processing in defining the ultimate limits in feature size, compositional and structural heterogeneity, and device performance.

The Future of Silicon Devices and Circuits

Electronic devices and circuits constructed from silicon materials have increased in performance and decreased in cost by a factor of 1 million during the last 35 years. Such an explosion of benefits is unparalleled in the history of any technology. Silicon materials have fueled the growth of the U.S. electronics industry to annual sales approaching $300 billion. The functionality made available by silicon components has created the information age.

Two driving forces are determining the course of applications for silicon materials. The most important is circuit integration, because, in the past, it has provided an exponential decrease in device cost with time. The second driving force is device speed. This is because the ability to move and analyze larger amounts of information has yielded new applications and markets and, hence, enhanced the value added to the raw material.

The role of materials and processes has been a matter of long-term concern. The unique properties of silicon were not universally available until the zone-refining process removed an overlay of defect and impurity effects.[1] Since that time, the use of vapor-phase purification techniques has become universal, but the confrontation among demands of device design, processing, and materials selection has continued unabated. However, the skepticism that once held that low-yield discrete devices could never be integrated into circuits as a single chip has given way to system integration at a level of 10^8 devices per chip! Today the limiting challenge is the integration of the process line to perform more than 500 fabrication steps with precision and congruency.

Materials and Processing Issues

Silicon technology is based on the electronic energy gap of silicon (E_g = 1.1 eV), which is ideal for room-temperature device operation, and a high-integrity oxide (SiO_2), which is used as an active dielectric, interconnection insulation, and process pattern mask. Active electronic interfaces are created by alloying (doping) and oxidation steps. These processes employ diffusion, ion implantation, thermal oxidation, and chemical vapor deposition (CVD). Device designers project limits to the current technology at lateral device dimensions of 1000 Å (angstroms), integration levels of 10^{10} devices per square centimeter, and operational times near 10^{-12} seconds. Beyond these limits, the market will demand greater functionality through increased chip size. This requirement translates into a need to lower defect densities and defect size by 13 percent per year with improved manufacturing processes and design.

The primary challenge in silicon technology today is *metallurgy*. Current materials systems are marginal in meeting the demands of high power dissipation, high-frequency operation, and high interconnect pin count. High-speed device performance has exceeded the *theoretical limits* posed by the resistance and capacitance of interconnection materials and layout.[2] The silicide and aluminum interconnect structures in current use must be replaced by higher-conductivity, patternable, and stable metal or intermetallic compound systems that are adaptable to complex multilevel structures. Tungsten, deposited by low-pressure chemical vapor deposition (LPCVD) for conformal coverage, is a prime candidate. Those who develop the appropriate interconnect technologies will be the major players in the silicon integrated circuit market in the year 2000.

Considerable attention has been given to merging the silicon and compound semiconductor technologies by using SiO_2 optical paths, which are free of resistance and capacitance limitations, as interconnect materials. However, on-chip integration of III-V compound light emitters and detectors on silicon has failed because of the high dislocation densities (greater than 10^8 cm^{-2}) resulting from the significant (more than 4 percent) lattice misfit between these materials and silicon. A similar limit is encountered in the integration of silicon-germanium alloys for high-speed device applications. In the past, each increase in integration level (components per chip) has been accompanied by an increase in chip size (area) and process complexity (number of process steps) and a decrease in defect density. If the trend in cost reduction and performance increase is to continue, the materials processing knowledge base must be extensive and its application must be innovative.

During the next decade the cost of a silicon processing line is projected to exceed $500 million. A modern facility is expected to generate $250 million/year

Acronyms and Abbreviations in This Paper

BICMOS	bipolar CMOS
CMOS	complementary metal oxide semiconductor
CVD	chemical vapor deposition
Ge	germanium
HBT	heterojunction bipolar transistor
IC	integrated circuit
LPCVD	low-pressure chemical vapor deposition
NMOS	n-channel MOS
MODFET	modulation-doped field-effect transistor
MOS	metal oxide semiconductor
PMMA	polymethyl methacrylate
PMOS	p-channel MOS
ppba	parts per billion atom fraction
SEG	selective epitaxial growth
Si	silicon
SiO_2	silicon dioxide
Ti	titanium
TiN	titanium nitride
ULSI	ultra-large-scale integration
VLSI	very large scale integration

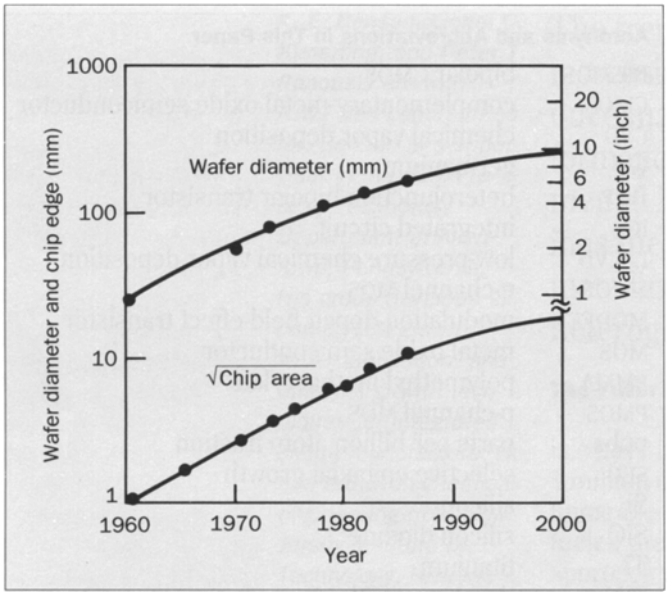

Figure 1. Historic trends in silicon wafer diameter and chip size with time. Functionality increases with chip size. Economic leverage in circuit fabrication is provided by increasing wafer size as the number of process steps increases.

in revenues. With the life of capital plant averaging less than 5 years, the incentive to compete is clearly decreasing. However, *the opportunity for a radical change in materials or manufacturing methods has never been so great.* (See, for example, Figure 3 in "Materials and Processing: Core Competencies and Strategic Resources" by C. K. N. Patel, pp. 2-8.) Those who remain at the forefront of materials research, development, and manufacturing will be the ones to reap the rewards of the integrated system chip revolution.

Silicon Preparation

Semiconductor (sometimes referred to as electronic-grade) silicon is the purest material ever made commercially in large quantities. Material is routinely produced with impurity concentrations of less than 1 part per billion atom (ppba) fraction (boron content less than 0.1 ppba, phosphorus less than 0.3 ppba, and carbon less than 0.5 ppma). Purity requirements for the ultimate levels of integration are projected to be less than 0.1 part per trillion atom fraction of stray contaminant atoms. Detection of such low levels is beyond current analytical capability. The control of impurities is one of the most important aspects in preparing silicon for semiconductor device applications.

Silicon Single-Crystal Growth. The basic requirement of bulk semiconductor silicon for device fabrication is single-crystal material with high crystalline perfection and the desired charge carrier concentration. The available commercial growers provide containment for a silicon charge size of 45 to 60 kg (kilograms) for growth of silicon crystals 125 to 200 mm (millimeters) in diameter. Silicon grower capacity has been scaled up in recent years, in proportion to the steady increase in crystal/wafer diameter as demanded by the economics of the integrated circuit (IC) manufacturing. Figure 1 shows silicon crystal/wafer diameter as a function of date of introduction of the technology. A 200-mm-diameter crystal grown from a 60-kg charge is not uncommon now. Experimental work at AT&T has shown that it is possible to grow dislocation-free, 300-mm-diameter crystals with proper thermal environment in which the thermal stress of the growing crystal is minimized (Figure 2). For high-volume production of large-diameter crystals, the logical extension of the batch process is the continuous-feed growing system involving one or more containers.

Wafer Process Technology. After the crystals (called ingots in the silicon industry) are grown, they are converted into polished wafers by machining and chemical processes. A selection of specifications for mechanical properties of a 150-mm-diameter wafer is shown in Table I. Structural, chemical and electrical parameters are specified on a silicon wafer used for leading-edge integrated circuit technology. The mechanical

Figure 2. Single crystal silicon ingots and wafers produced at AT&T Bell Laboratories. The polished wafers are 175, 200, and 300 mm in diameter, respectively. (From K. E. Benson and W. Lin, AT&T Bell Laboratories, Allentown, Pennsylvania.)

dimensions are based on processing requirements, capabilities of the various shaping equipment, and cost objectives. The tolerances are among the tightest for any formed object, and they shrink with each succeeding generation of technology.

Silicon Epitaxial Deposition. The deposition of single-crystal silicon layers upon silicon substrate wafers (referred to as epitaxial deposition), has been a principal processing tool since the early days of silicon technology. This deposition process allows the device designer the flexibility of having a lightly doped region in which to fabricate the active device, directly above a uniformly, or selectively, heavily doped substrate. This multilayer structure provides enhanced electrical performance over simply constructing the device in a uniformly doped single crystal wafer. Epitaxial layers range in thickness from 0.03 μm to more than 100 μm, with growth rates varying from 0.001 to 5 μm/min, and with deposition temperatures spanning the range from 500 to 1250°C.

Table I. Selected Mechanical Specifications for a 150-mm-Diameter Silicon Wafer

Thickness	675 ± 25 μm
Total thickness variation	5 μm
Flatness (focal plane deviation)	≤ 0.4 (± 0.2) μm
Particles	0.1 cm^{-2}, > 0.2 μm in size

The growth of sharp, multilayered structures, where the layer boundaries are defined by a difference in dopant level or type, is difficult to obtain using conventional epitaxial chemical vapor deposition (CVD). This limitation is due to system transients in both the silicon source and the dopant species. Solid-state diffusion also plays a role in dopant transport, causing smearing of the interface regions at typical deposition temperatures. Low-pressure, low-temperature CVD in an ultrahigh-vacuum chamber will be used to probe the limits of materials and process control of the CVD technology.

Lateral separation of adjacent regions in VLSI circuits is limited by the isolation procedures used. Selective epitaxial growth (SEG) (see Figure 3), allows the deposition of single-crystal silicon into regions defined by a SiO_2 layer. The SEG process suffers from faceting; (311) facet planes become evident along the [110]

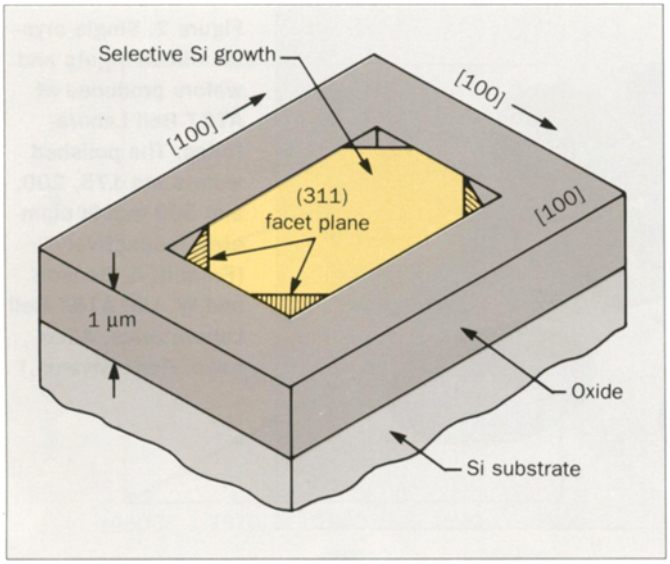

Figure 3. Sketch of a selective epitaxially grown silicon layer. The layer geometry is initially defined by the silicon dioxide window dimensions. As the layer thickens, the slow-growing crystallographic faces control the shape.

directions for (100) oriented layers greater in thickness than about 0.5 μm. These facets limit the amount of planar silicon surface area and also complicate coverage of these selective regions with subsequent layers.

Silicon epitaxial deposition will continue to be a major processing technology for the production of VLSI and ULSI devices. The use of epitaxy in CMOS devices is increasing, while the wafer cost is being reduced. Lower defect levels, reduced contamination levels, SEG and improved dimensional control (minimization of flatness degradation) are the major frontiers.

Silicon-Germanium Heterostructures. Heterostructures for devices utilize sandwiches of different material compositions to enhance performance. Germanium and silicon are isoelectronic and completely miscible, but their difference in atomic size gives a crystal

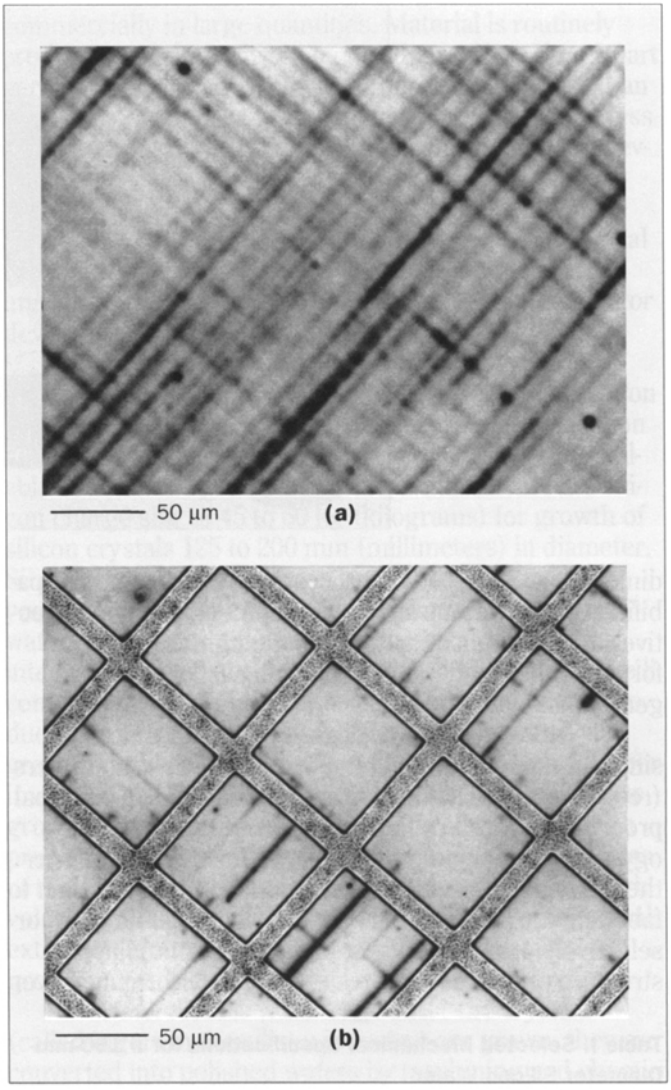

Figure 4. Electron micrographs of a 2800-Å-thick $Si_{0.81}Ge_{0.19}$ layer on Si. (a) Large area growth containing a high density of misfit dislocations; (b) growth on 70-μm-wide silicon mesas with a reduced dislocation density.[3]

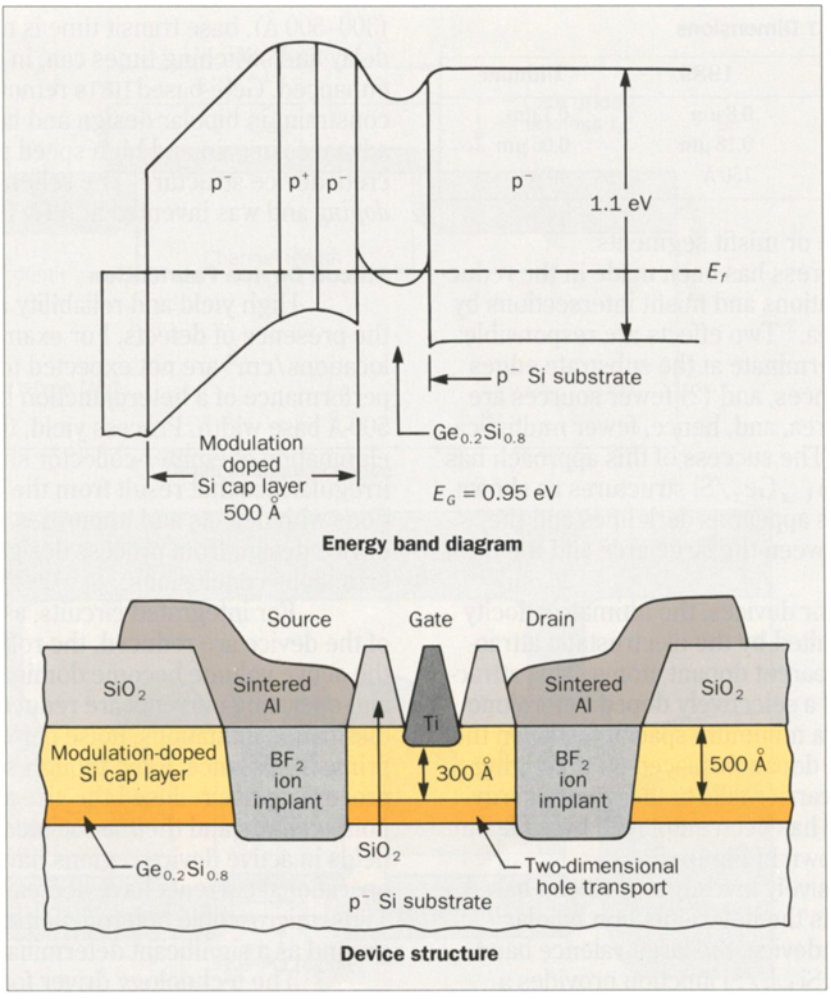

Figure 5. Energy band diagram and schematic device structure of the p-channel, modulation-doped field effect transistor (MODFET) fabricated by AT&T Bell Laboratories.[4]

lattice mismatch of 4.2 percent. In the case of mismatched interfaces, the layer strain is given by the misfit

$$f = (a_s - a_0)/a_0 = \varepsilon + \delta$$

where a_s is the lattice parameter of the substrate, a_0 is the relaxed lattice parameter of the film, ε is the elastic strain and δ is the plastic strain.

Plastic strain is accommodated by misfit dislocations which must terminate at a surface (the edge of the layer or in the growth plane). Thus, one distinguishes between two types of dislocations: *misfit dislocations* that form a *planar* array to relieve strain at or near the interface and *threading dislocations* that propagate into the

Table II. Scaling of MOSFET Dimensions

Date	1960	1989	Ultimate
L_{min}	25 μm	0.8 μm	0.1 μm
X_j	5 μm	0.18 μm	0.05 μm
t_{ox}	1000 Å	150 Å	40 Å

epilayers from substrate or misfit segments.

Significant progress has been made in the reduction of threading dislocations and misfit intersections by reducing the growth area.[3] Two effects are responsible: (1) misfit dislocations terminate at the substrate edges after gliding short distances, and (2) fewer sources are contained in a smaller area, and, hence, fewer multiplication interactions occur. The success of this approach has been demonstrated in $Si_{1-x}Ge_x/Si$ structures as shown in Figure 4. Dislocations appear as dark lines and the reduction in density between the large area and the mesa patterns is clear.

In semiconductor devices, the ultimate velocity of a charge carrier is limited by the electrostatic attraction between it and the parent dopant atoms. This attraction can be minimized if a selectively doped heterojunction is used to maintain a minimum spacing between the dopant and carrier. The dopant is placed on the higher band gap side, and the carrier falls to the lower energy side. This configuration has been employed by AT&T in MODFET devices[4] as shown in Figure 5.

The most intensively investigated silicon-based heterostructure device is the heterojunction bipolar transistor (HBT). In this device, the large valence band discontinuity of the Ge_xSi_{1-x}/Si junction provides a natural barrier to the back emission of holes from the p-type transistor base into n-type emitter. As such, the gain of the device can be maintained as the base doping is increased 1-2 orders of magnitude above that in the corresponding homojunction transistor. The higher doping decreases the resistivity of the base layer, allowing the use of much thinner bases with acceptable lateral series resistance. In such thin base structures (300–500 Å), base transit time is no longer the limiting delay and switching times can, in principle be greatly enhanced. GeSi-based HBTs remove a significant design constraint in bipolar design and have already yielded advances in gain and high speed performance of the discrete device structure. The scheme is called *modulation doping* and was invented at AT&T Bell Laboratories.[5]

Silicon Device Fabrication

High yield and reliability are not compatible with the presence of defects. For example, 10^5 threading dislocations/cm^2 are not expected to impair electrically the performance of a heterojunction bipolar transistor with a 500-Å base width. Process yield, though, is dependent on elimination of emitter-collector shorts and junction depth irregularities that result from the interaction of dislocations with defects and impurities. The separation of device design from process design can clearly lead to erroneous conclusions.

For integrated circuits, as the lateral dimensions of the device are reduced, the role of individual defects in the active volume become dominant. As bias voltages and operating currents are reduced for reasons of power dissipation limitations, noise performance will assume prime importance. Even though sophistication in device processing has reduced the size and density of potential noise centers and their associated currents, the electric fields in active device regions have increased and the operational currents have decreased with device scaling. Thus, microscopic heterogeneities arise from the background as a significant determinant of yield and reliability.

The technology driver for ICs has been the metal-oxide-semiconductor field-effect transistor (MOSFET) device. As a planar structure, this device offers advantages in dimensional definition and control during processing. As a majority carrier device, it has a greater immunity to material defects than bipolar, minority carrier devices. Integrated circuit design pairs n-channel (NMOS) and p-channel (PMOS) devices for optimum packing density in a complementary (CMOS) design. For

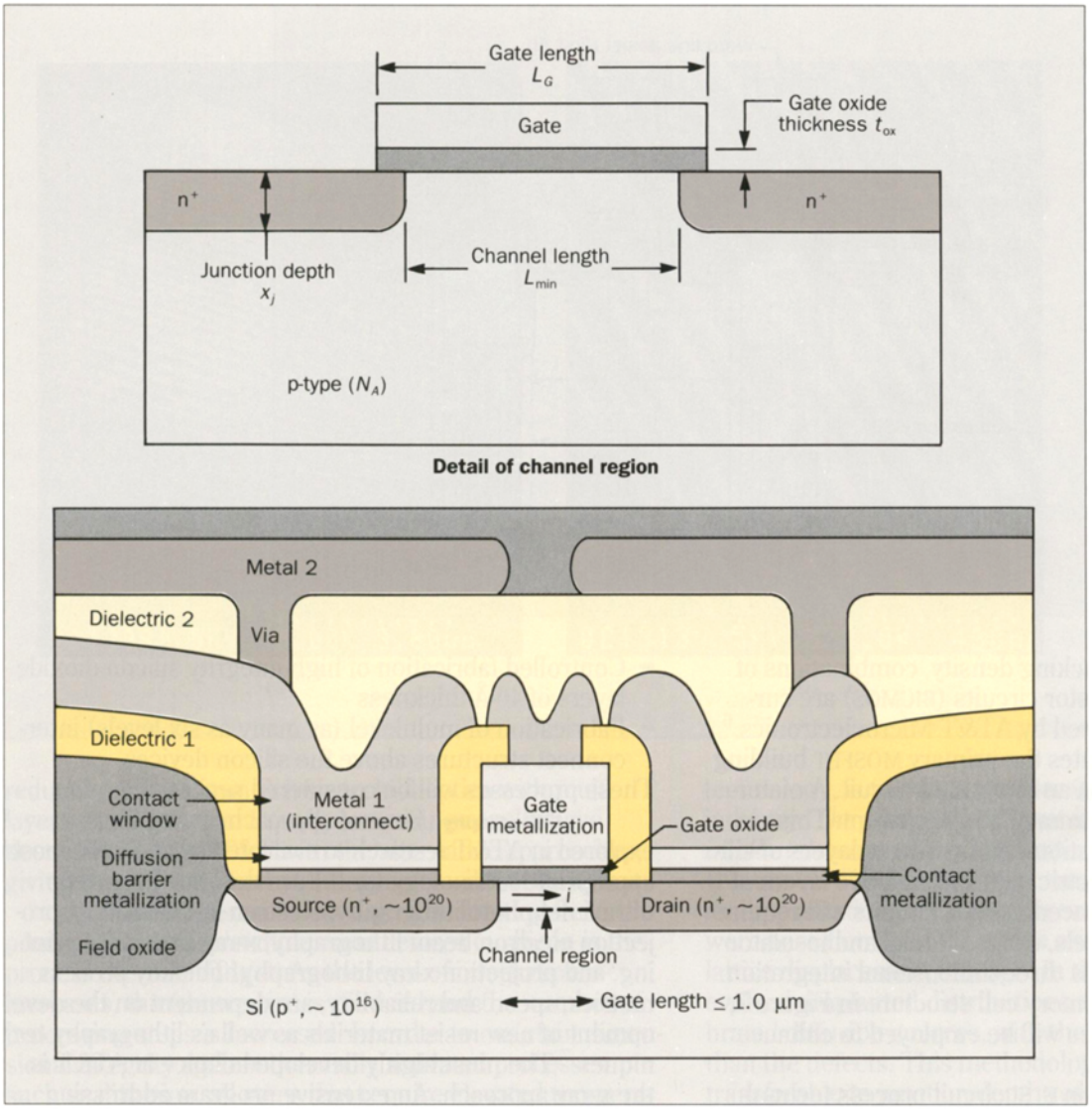

Figure 6. Diagram of a cross section of an n-channel MOSFET device indicating the many layers of different materials. Shown are three layers of silicon, four dielectric layers, and five layers of metal. The detail diagram shows the critical dimensions that determine process technology scaling, as given in Table II.

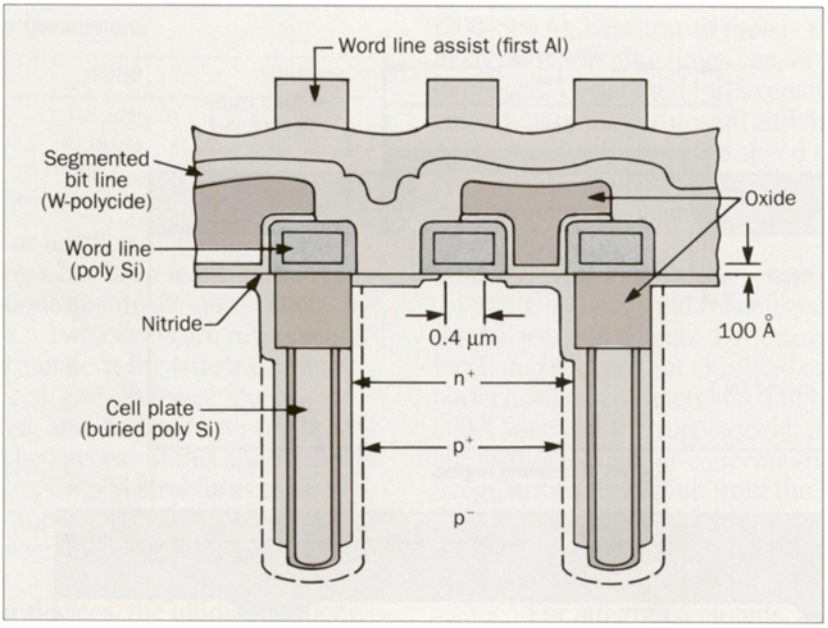

Figure 7. A schematic memory cell structure for the 0.35-μm design generation. Note that vertical trenches are employed to improve wafer area utilization.

reasons of speed and packing density, combinations of bipolar and MOS transistor circuits (BICMOS) are currently being manufactured by AT&T Microelectronics.[6]

Figure 6 illustrates the primary MOSFET building block as implemented in an integrated circuit. A materials integration issue is immediately apparent. This elementary stage of integration employs three layers of silicon, four layers of dielectric material, and five layers of metal. Bipolar and advanced BICMOS circuits will require up to four additional levels, each, of metal and insulator materials. A final trend is three-dimensional integration. As illustrated by the memory cell structure in Figure 7, vertical trench structures will be employed to enhance utilization of wafer area.

The key issues in ULSI circuit process technology are:

- Lithography and pattern transfer of small dimensions (0.1 μm)
- Production of shallow junctions (500 Å)
- Controlled fabrication of high-integrity silicon dioxide layers of 40-Å thickness
- Fabrication of multilevel (as many as six levels) interconnect structures above the silicon devices

These processes will be considered separately.

Lithography. Several approaches are being explored in AT&T research to evaluate and apply the most appropriate technology for 0.1-μm design rules: deep ultraviolet photolithography, electron-beam writing, projection electron-beam lithography, x-ray proximity printing, and projection x-ray lithography. The key process metrics, speed and reliability, are dependent on the development of new resist materials as well as lithography techniques.[7] The most highly developed choice at AT&T is the x-ray approach. An extensive program addressing sources, mask fabrication, and performance began in the early 1980s. Recent work has focused on the critical area of x-ray optics for reduction printing. Figure 8 shows a series of 0.05-μm lines and spaces produced with a 20:1

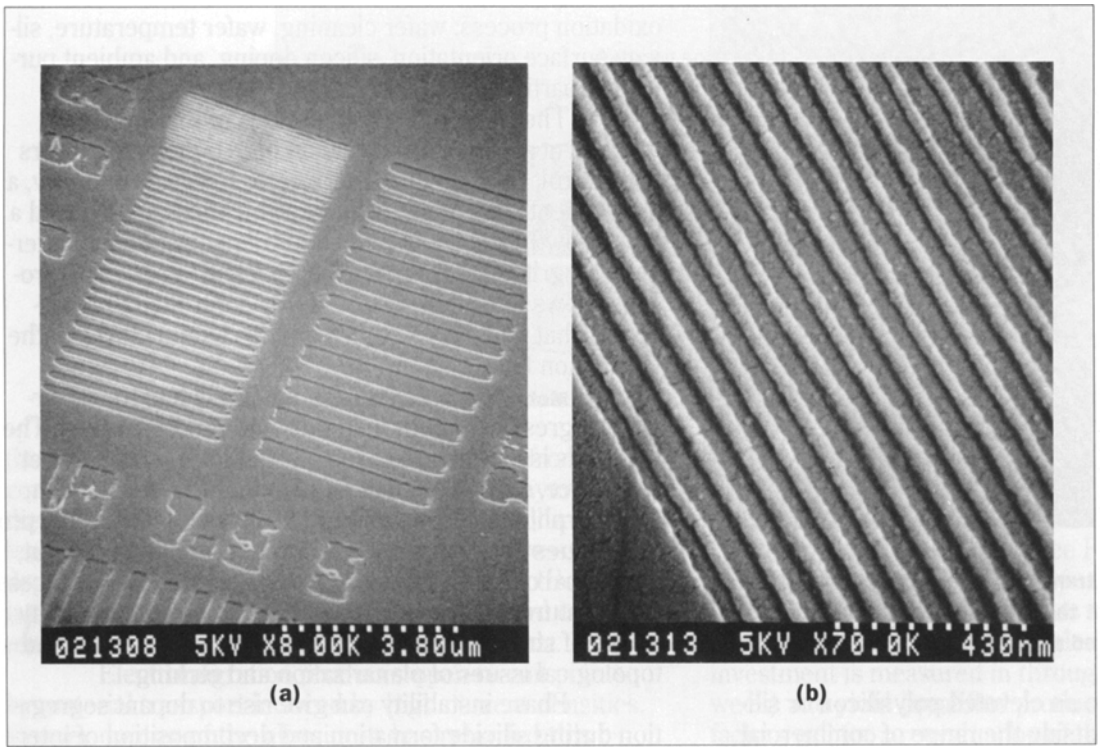

Figure 8. A series of 0.05-μm lines and spaces produced by projection x-ray lithography with a 20:1 reduction and recorded on polymethyl methacrylate (PMMA) (by R. R. Freeman).

reduction image from Schwartzchild optics with multilayer coated mirrors. Equally promising results have been achieved at AT&T with the alternative approaches, giving the impression that lithography will not be a limit.

Shallow Junction Processing. The limiting factor in producing submicron-dimension devices in silicon is the process thermal budget. As the level of integration increases, the feature size is reduced and the number of processing steps is increased. In order to maintain dimensional integrity against thermally activated processes such as diffusion, all steps that require elevated temperatures must fit within a tight thermal budget.

Ion implantation is the key technology for junction profile control. The alternative of doped epitaxial growth, as is practiced in compound semiconductor technology, is too expensive for the cost-driven silicon industry. *The fundamental limit is the complete removal of implant damage with no accompanying dopant diffusion* (Figure 9). The primary objections to the installation of ion implantation in silicon processing in the early 1970s were based on the deleterious effects of the associated lattice displacement damage. In the technology that has evolved, implanted distributions are used as highly calibrated diffusion sources, with the junction lying deeper than the defects. This methodology is clearly not directly transferable to junction depths of 500 Å.

The shallow junction processes under current development are (1) low-energy implantation ($E < 10$ keV) into crystalline silicon, (2) low-energy implantation into a preamorphized silicon surface layer,

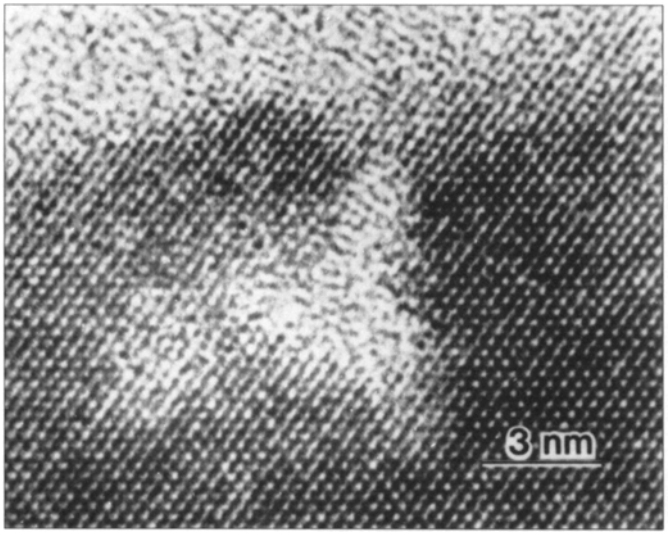

Figure 9. High-resolution transmission electron micrograph of end-of-range damage at the crystal/amorphous boundary in 200 keV $^{28}Si^{+}$ implanted silicon: [011] zone axis image.[8]

and (3) implantation into an elevated polysilicon or silicide film. Process 1 is outside the range of commercial implantation equipment and is limited by ion channeling and defect-enhanced diffusion. Process 2 is capable of producing junction depths of $x_j \geq 0.1$ μm. Process 3 is favored for $x_j < 0.1$ μm, because a silicide or metal cladding is required in device design to reduce sheet resistance. In all three cases, interfaces play a dominant role in determining process quality.

Gate Oxide Growth. The smallest dimension in a MOSFET is the gate oxide thickness. At the projected limit of 40 Å, both the oxidation temperature and ambient temperature are critical. Uncontrolled growth of the native oxide on silicon at room temperature on exposure to air produces a layer about 15 Å thick. Production of uniform active dielectric layers of less than 100-Å thickness is not possible with today's technology. Absolute control of the following parameters is considered critical to the gate oxidation process: wafer cleaning, wafer temperature, silicon surface orientation, silicon doping, and ambient purity and partial pressure of oxygen.

The narrow process margins of this step have initiated at AT&T the integration of CVD dielectric layers for control. A thin oxide is grown for interface integrity, a subsequent layer is deposited for thickness control and a final growth step is performed for densification and interface integrity (Figure 10). This "stacked" gate oxide process allows for the design of highly controlled unit processes that may be combined at different junctures in the fabrication line.[9]

Metallization. Metallization limits integrated circuit progress with both materials and process issues. The materials issues are phase stability at interfaces, contact resistance, series resistance of interconnects, adhesion, and morphology for submicron feature definition. The process issues are selective deposition for high throughput, conformal coverage of high-aspect-ratio vias, wide process temperature windows, layer thickness control, reliability issues of stress-induced voids and electromigration, and topological issues of planarization and etching.

Phase instability can give rise to dopant segregation during silicide formation and decomposition of interconnect materials. This problem has been addressed primarily by the installation of intervening diffusion barriers (Ti, TiN). Electrical properties of interconnects are undergoing generational changes from polycrystalline silicon to silicide compounds to metals. The current standard of aluminum may be superseded by tungsten because of AT&T's tungsten CVD process. CVD has advantages over sputtering and evaporation for conformal coverage in deep vias. For lines below 0.4 μm, the enhanced conductivity of copper may be required. The close spacing of the conductor lines has posed an additional capacitance limitation to circuit speed.[2] To maintain the growth in integration level, low-dielectric-constant interlevel insulators will be required.

Open-circuit points on aluminum metallization lines result from material transport induced by stress in

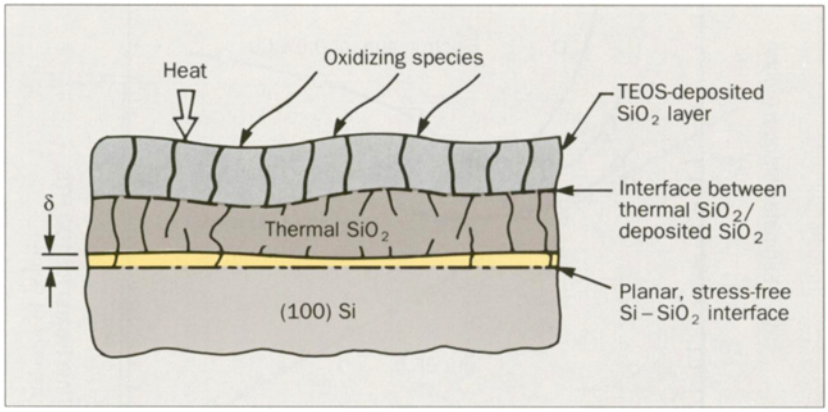

Figure 10. Schematic cross section of a "stacked" gate oxide structure, which provides high-performance, thin-gate dielectrics.[9] The diagram illustrates the role of heat treatment in an oxidizing ambient to create an "electronic grade" $Si-SiO_2$ interface.

the metal film. These stresses arise primarily from the compressive state of the interlevel dielectric layers. Studies show that the higher the number of metallization levels, the more uncontrollable is the layer stress. Better deposition processes for both metal and dielectric materials are required, with materials selection based on mechanical as well as electrical property criteria.

Electromigration produces open-circuit points by material transport induced by high current densities. Copper doping of the aluminum has retarded this mechanism. Work at AT&T has revealed a critical role of grain structure.[10] Figure 11 shows that, as interconnect lines become narrower, a "bamboo structure" appears that does not contain vulnerable triple-point grain boundary intersections. Thus, the reliability increases with reduced feature size. The grain structure of the initial film is also important. Both tungsten and copper interconnects are expected to have an increased resistance to electromigration because of their lower atomic diffusivity at device operating temperatures.

The Silicon Fabrication Line

Three trends are evident in the evolution of materials and processing with increasing integration level: (1) increasing heterogeneity built into the silicon and in overlayers, (2) lower processing temperatures, and (3) more and varied materials and processes.

Increases in integration level have required increased capital investment to handle the more sophisticated process technologies (see Figure 12a). The success of a silicon IC business depends critically on leveraging volume production and sales against the high capital cost of plant facilities. The efficiency of a given plant investment is measured in throughput (wafer starts per week) and yield (qualified product per wafer lot). Five factors call for a reevaluation of the state-of-the-art fabrication line concept:

- *Customization and throughput*: the product mix is expanding, and a generic clean room layout and set of unit processes is becoming inefficient.
- *Turnaround time*: there is a need to decrease the time for wafer flow through fabrication in order to optimize chip design and processing to meet market demands.
- *Wafer size*: the industry standard wafer diameter will soon exceed 8 inches (200 mm), and single-wafer processing will be introduced for homogeneity and control.
- *Process complexity*: these conflicting demands require simplified, robust processes with a rapid evolution in process and handling cleanliness.
- *Capital investment*: the high cost of plant will limit semiconductor technology before physical limits unless a radical change in materials processing and

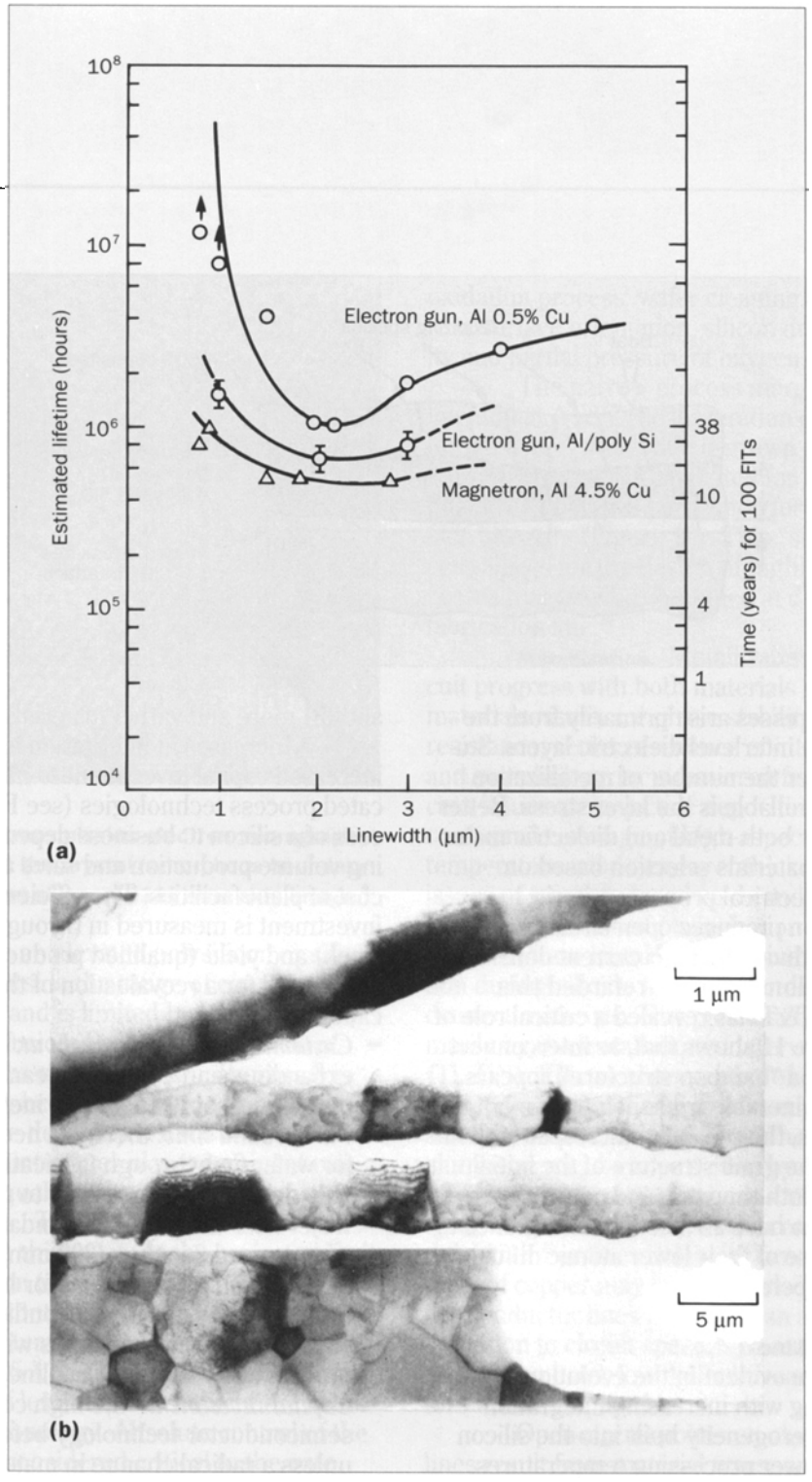

Figure 11. The correlation of reliability of interconnect lines with grain structure. (a) The unexpected result that lifetime increases for conductor line widths below 2 μm. (b) Transmission electron micrographs showing that narrow linewidth conductors possess single-grain microstructures that exhibit reduced electromigration.[10]

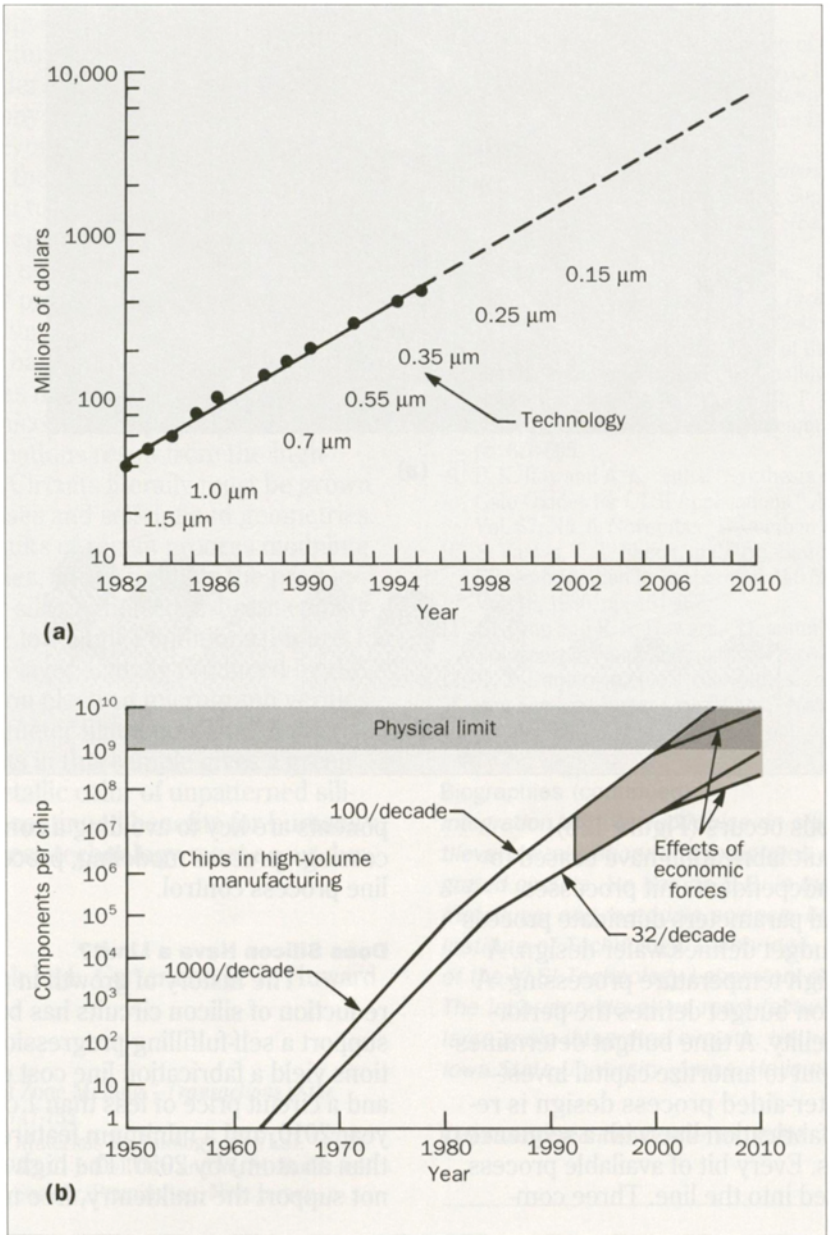

Figure 12. The role of economic forces in reaching the limits of silicon processing. (a) Increasing capital outlay for a fabrication line with increasing process sophistication; (b) interaction of physical limits and economic limits in defining evolution of circuit integration level (from D. L. Carter).

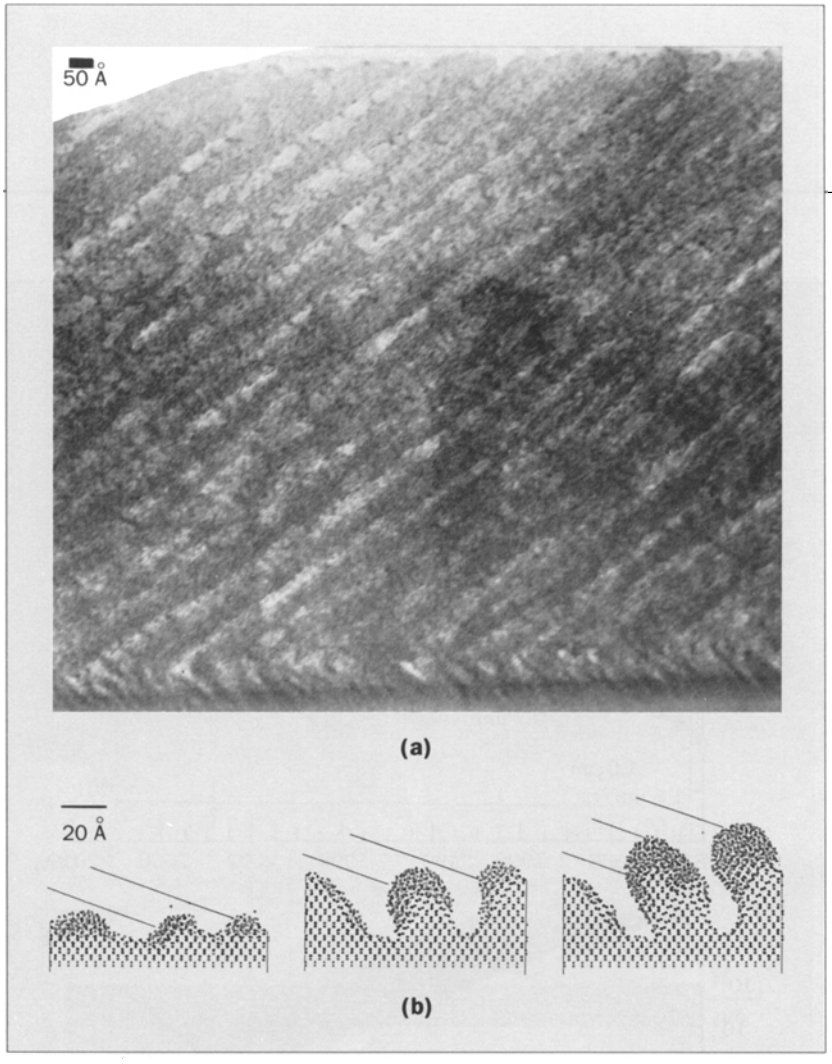

Figure 13. Self-regulated definition of 50-Å silicon filaments by low-angle molecular-beam epitaxial deposition. (a) Transmission electron micrograph of filaments; (b) schematic diagram of the deposition process. (From G. H. Gilmer, E. A. Fitzgerald, and Y.-H. Xie.)

manufacturing methods occurs (Figure 12b).

Device and circuit fabrication have ceased to exist as a sequence of independent unit processes. Tight budgets for critical parameters dominate process design. A mechanical budget defines wafer design. A thermal budget limits high-temperature processing. A particulate/contamination budget defines the performance of the process facility. A time budget determines the acceptable throughput to amortize capital investment. Accurate computer-aided process design is required on an advanced fabrication line with a sequence of 300 to 500 process steps. Every bit of available process margin must be squeezed into the line. Three components are key to avoiding a complexity limit to IC processing: process modeling, process monitoring, and on-line process control.

Does Silicon Have a Limit?

The history of growth in performance and cost reduction of silicon circuits has bred the confidence to support a self-fulfilling progression. Current extrapolations yield a fabrication line cost of more than $1 billion and a circuit price of less than 1 cent per megabit by the year 2010, and a minimum feature size of 1 Å (smaller than an atom) by 2050. The high capital investment cannot support the multientry, free market industry that

exists today. The alternatives are drastic process simplification or a foundry structure in which a few sites process for many vendors. In order to reach the performance goals, both new device physics and new concepts in processing are required. Beyond today's device technology and logic structures lies the possibility of devices based on quantum confinement to contain electrons in regions dimensioned in tens of angstroms.[11] Combined with cellular automata concepts to perform memory and logic functions, this approach may provide the means to breach the limits seen for extrapolating the state of the art.

The knowledge base in materials and processing for quantum circuits does not exist. Recent research on 20- to 40-Å-diameter semiconductor particles reveals that new structural transformations result from the high surface/volume ratio.[12] Circuits literally must be grown with self-limiting processes and self-defined geometries. Figure 13 shows the results of recent process modeling at AT&T Bell Laboratories, which predicts the production of 50-Å filaments by silicon molecular-beam epitaxy deposition under unique low angle conditions. Figure 13a is a picture of the silicon layer actually produced by the process. The transmission electron micrograph verifies the presence of 50-Å-diameter filaments. The interaction of light with the filaments in this sample gives a green color rather than the metallic color of unpatterned silicon. If silicon is to yield continued benefits for humanity, a true revolution in process technology must occur during this decade.

Acknowledgment

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