POLYMERS IN ELECTRONICS PACKAGING

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Integrated circuit packaging affects component performance, price, and reliability. Molded plastic packaging is cost-efficient compared to other packaging processes, and offers both quality and reliability. In recent years, AT&T Microelectronics has made significant improvements in package quality through a closely monitored quality program. Rapidly evolving device technology will make new demands on packaging to accommodate increases in device speed, miniaturization, and power dissipation. Packaging and interconnection will continue as significant factors affecting further advances in system performance. AT&T's expertise in packaging sophisticated, high lead-count devices has been achieved by focused development efforts and a packaging research program. New materials and process technology help AT&T package development engineers realize advanced designs for customer needs. Several new packaging technologies—including multichip modules, tape-based packages, and optical interconnection—will emerge in years to come, and could radically change the nature of packaging. AT&T will meet its customers' needs in microelectronics packaging by staying at the forefront of packaging design, materials and process technology.

Introduction

The packaging of an electronic component profoundly affects its performance and reliability. Plastic packaging—the low cost option for reliable, high quality devices—accounts for almost 90 percent of the 30 billion devices packaged annually worldwide. Plastic packaging, including assembly and testing, represents as much as 40 percent of the component's cost, and its features and cost affect its competitiveness.

Panel 1. Terms and Acronyms in This Paper

AOQ	average outgoing quality
CCC-DCA	leadless ceramic chip carrier with direct chip interconnection
CCC-WB	leadless ceramic chip carrier with wire bonding
CTE	coefficient of thermal expansion
DIP	dual in-line package
FEA	finite element analysis
HIC	hybrid integrated circuit
IC	integrated circuit
I/O	input/output
leadframe	an assembly of fan-out patterns for several packages attached together in a strip that has been either punched or etched
MCM	multichip module
MOS	metal oxide semiconductor
PAA	polyamic acid
PGA	pin grid array
PLCC	plastic leaded chip carrier
PMDA-ODA	pyromellitic dianhydride-oxydianiline polymide
PMP	plastic multilayer packages
PQFP	plastic quad flat package
QA	quality assurance
QFP	quad flat package
TAB	tape automated bonding

Wafer fabrication—not packaging—has been the rate-determining aspect of silicon integrated circuit (IC) performance and miniaturization, and has been the focus of most R&D efforts. Despite the limited investment in R&D into packaging, plastic packaging technology has made it possible for nearly all devices, except those used in specialized applications, to be packaged at low cost. This technology has promoted the use of chips in a wide array of consumer products. The rapid evolution of device technology is making packaging and interconnection (i.e., the overall communication between a computer chip and the system) an ever-increasing determinant of systems evolution.

AT&T committed more than 10 years ago to extensive use of plastic in packaging highly sophisticated silicon devices. Although AT&T was a latecomer to the technology, focused research and development efforts have given it a technical edge. The packaging effort took advantage of and complemented AT&T's silicon product mix, which emphasizes higher lead counts and more sophisticated devices when compared to the rest of the industry. Thus, AT&T was among the first to encounter and resolve problems associated with higher lead counts, higher silicon-to-package area ratios, and higher heat dissipation.

However, significant challenges lie ahead. As older packaging technologies such as wire bonding reach their limits, they will be replaced by new designs and processes such as tape technology-based packages, active thermal management structures, and optical interconnection. The challenge is to know the limitations, predict the emerging technologies, and put them into practice before the competition. In this way, the present limits represent an opportunity for a supplier to differentiate itself from its competitors. Component manufacturers who can retain low cost plastic packaging when others must resort to more expensive ceramic and premolded packaging options will enjoy a distinct competitive advantage in the marketplace.

Types of Packages

Packaging has five basic functions:

- Physical protection from the environment
- Interconnection to the next signal level
- Signal propagation matching
- Thermal management
- Providing a mechanically precise exterior to aid in testing, handling and assembling the component into electronic systems.

Most packages consist of electrical leads inter-

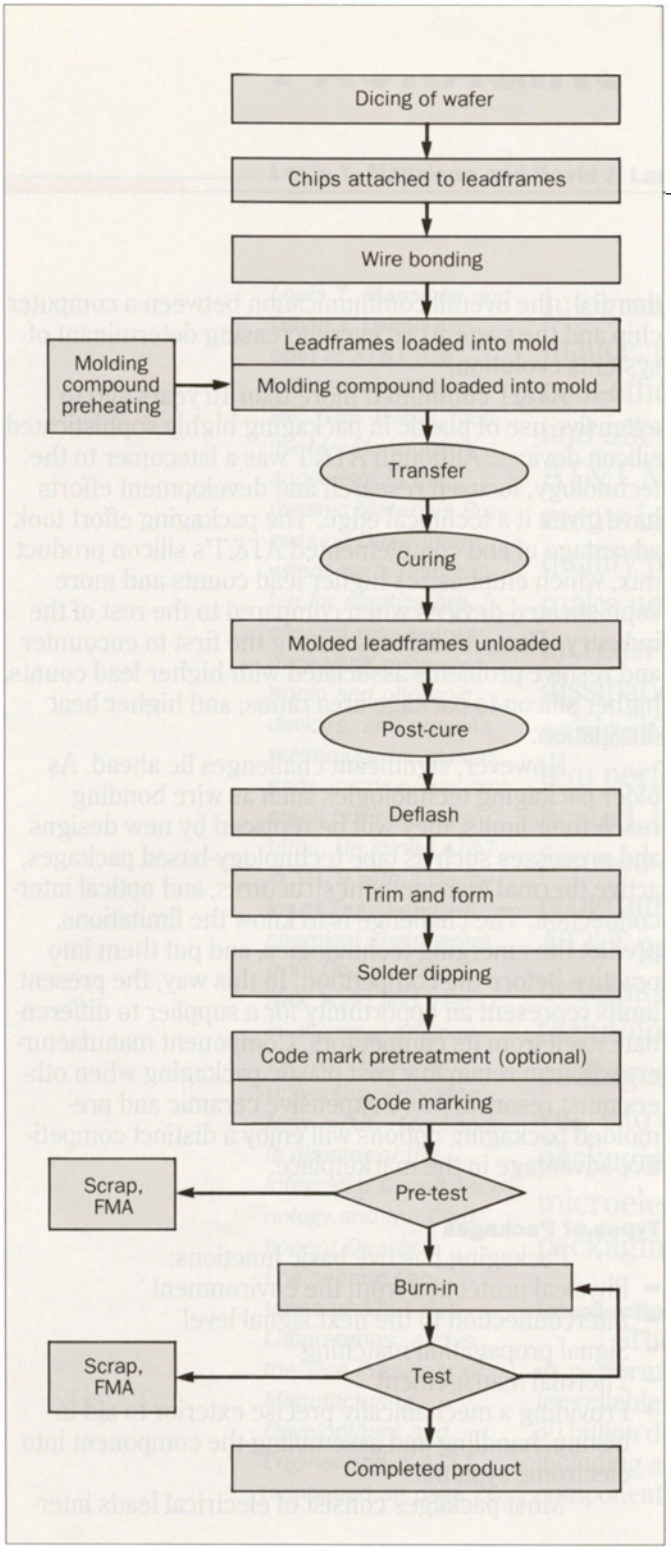

Figure 1. A flow chart showing the process steps in molded plastic packaging. Different manufacturers may use a different order of process strips.

connecting the small bond-pad spaces of the device to the larger lead spacings that can be accommodated by the next higher level of interconnection (e.g, a printed circuit board). Packages can also include power and ground distribution planes, internal interconnection patterns, and thermal dissipation structures. Package leads are supported or encapsulated in a package body. They protrude from the package and are attached to the bonding sites of the printed wiring board.

There are several major package types used by AT&T and the electronics industry. These include ceramic, refractory glass, pre-molded plastic, and post-molded plastic.

Ceramics. Ceramic packages are constructed by building up layers of ceramic precursor tape (a clay-like material that becomes ceramic after firing), adding the metal interconnect lines that often pass between the layers, then firing the assembly to form the package body. The device is mounted in a recess in the ceramic body, and is attached to the fan-out pattern either through wire bonds or a direct chip attachment method. A metal or ceramic lid seals the structure. Ceramic packages are usually hermetic and are presumed to offer higher reliability than nonhermetic packages, although the difference is decreasing. Ceramic packages are also excellent heat dissipaters. Packages made from refractory glass technology are also an option. They are not as expensive to make as ceramic packages because they are based on leadframes. (A *leadframe* is an assembly of fan-out patterns for several packages attached together in a strip that has been either punched or etched.) Both ceramic and refractory glass packages are less than 10 percent of the worldwide total; and this fraction is decreasing as ICs are used in more consumer products.

A pre-molded plastic package is similar to a ceramic package in that the device is mounted in the recess of a prefabricated body. These nonhermetic

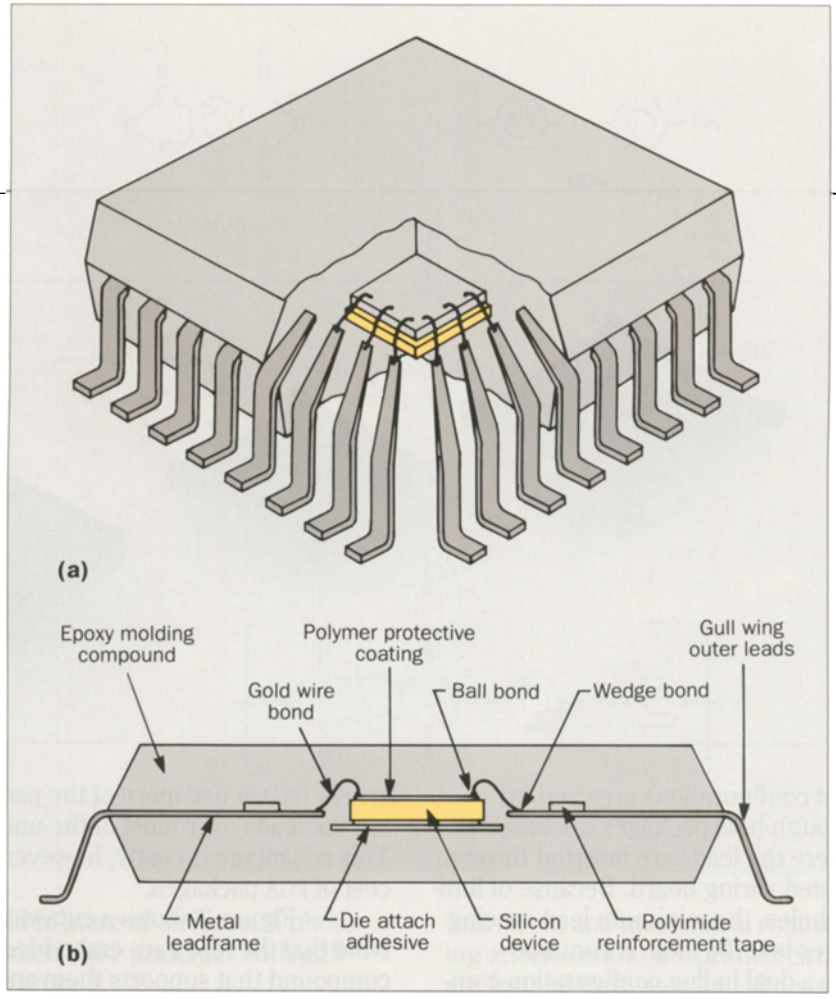

Figure 2. Cut-away (Figure 2a) and cross section (Figure 2b) views of a plastic quad flat package (PQFP), a surface mount, molded plastic package. The principal materials used in the package are shown.

packages are sometimes necessary to accommodate very high lead count devices, or to provide plastic pin grid arrays that are more difficult to mold. They account for only a small but important fraction of market share. Prefabricated packages based on multilayer printed wiring board—known as plastic multilayer packages (PMP)—are an important option for packaging high lead count devices that cannot be handled with post-molding.

Post-Molded Packages. Most plastic packages are post-molded, meaning the package body is molded over the assembly *after* the device has been attached to the fan-out pattern. This allows assembling and processing on leadframes with as many as 12 device sites per leadframe strip. Twenty or more leadframe strips can then be encapsulated in a production-size molding tool over a three minute cycle to provide high productivity and a low-cost package. Of the 3-minute cycle time, the plastic molding compound flows into the mold in 15 seconds; two minutes is needed to polymerize or cure the plastic; and the remaining time is used to prepare the mold for the next molding cycle.

Following molding, a plastic package requires some secondary operations, such as a large batch post-cure (or post-polymerization) to complete the polymerization reaction. The packages are then separated from the leadframe strip, and the leads are formed to their final configuration in a *trim and form* operation. Other secondary operations include writing information on the package with either inks, lasers, or plating; full function testing; and an "infant mortality" screening known as *burn-in*, where the device is operated at elevated temperatures and bias to eliminate premature failures. The steps involved in molded plastic packaging are described in the flow chart in Figure 1.

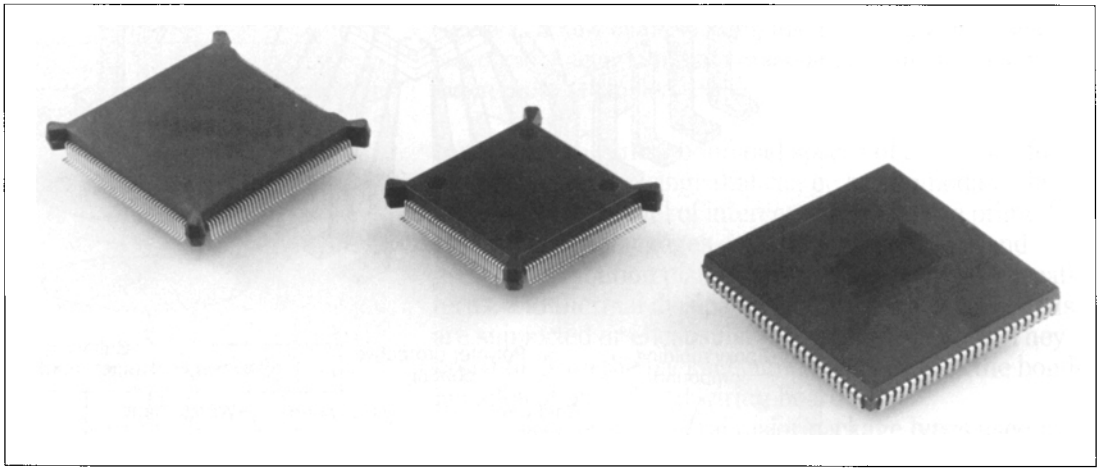

Figure 3. Photograph of three PQFP packages with gull wing leads on 0.025 inch outer lead pitch. The lead counts shown are 84, 100, and 132.

Several different configurations are used in molded packaging. Through-hole packages are based on an older technology where the leads are inserted through the interconnecting printed wiring board. Because of limitations in drilling these holes, the minimum lead spacing on through-hole packages is 0.100 inch. A common through-hole package is a dual in-line configuration commonly known as a DIP (dual in-line package). Although DIPs now account for a large fraction of the overall share of package types, they are losing ground to surface mount packages such as the plastic leaded chip carrier (PLCC) and the plastic quad flat package (PQFP). [Quad flat packages (QFPs) are similar to PQFPs, but do not have corner bumpers to protect the leads.] Surface mount packages do not have the restrictions of minimum lead pitch that through-hole technology creates, and they have the added advantage of being able to mount components on both sides of the board. PQFPs often incorporate finer outer lead pitch: 0.025 inch or less, compared to the standard 0.050 inch pitch of PLCCs. All three package types discussed so far—DIPs, PLCCs, and PQFPs—incorporate leads along the periphery of the molded body. This is a limitation because it crams the interconnection onto the thin outline of the package rather than throughout the package area. Pin grid arrays (PGAs) use more of the package area by dispersing the leads over most of the underside of the package. This advantage is costly, however, because of the higher cost of PGA packages.

Figure 2 shows a cutaway view of a QFP package. Note that the leads are embedded in the plastic molding compound that supports them and provides electrical isolation. The lead tips close to the chip are known as the *inner leads*. They are connected to the bonding pads through fine gold wire bonds. The outer leads are formed for mounting on the circuit board. This pitch (i.e., spacing between the leads) determines the overall package size; thus, there is strong motivation to minimize this spacing with the trade-off that finer pitch is more difficult to attach to the board with the near perfect yields required.

Two types of leads are used with surface mount packages:

- *"J" leads.* These are tucked under the molded body, conserve area on the circuit board, but are difficult to inspect.
- *Gull wing leads.* These are formed away from the molded body, and allow visual inspection of the solder attachment to the printed circuit board.

Fine pitch PQFP packages typically use gull wing leads,

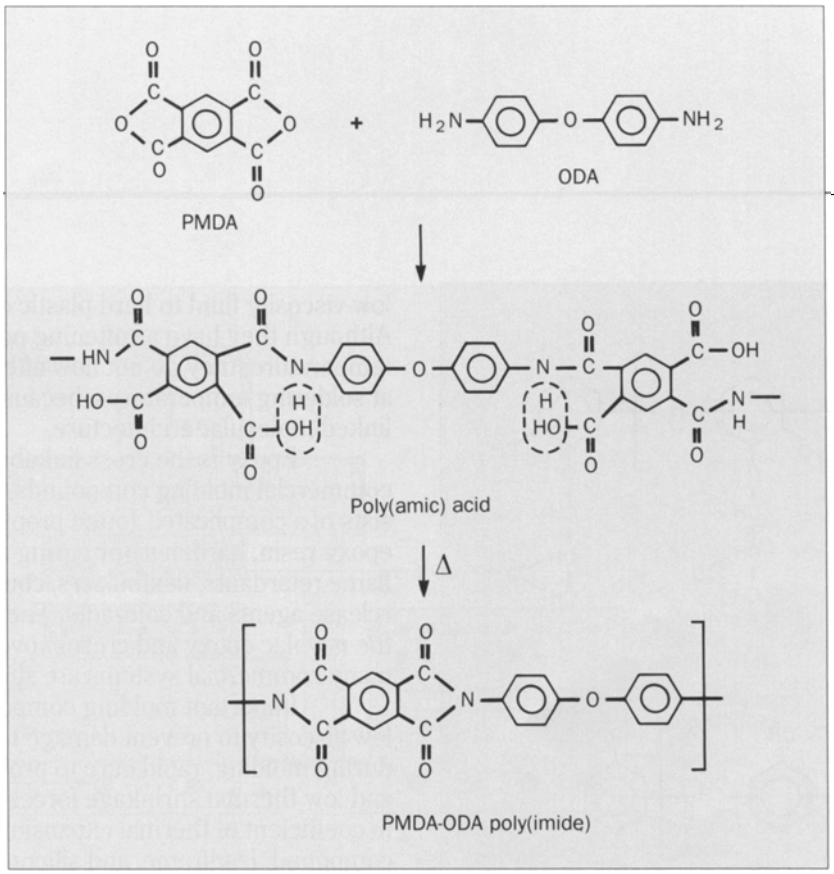

Figure 4. Chemistry and structure of PMDA-ODA polyimide, a material used as an interlayer dielectric or a protective coating on the device.

because attachment yield is more of an issue. A photograph of the three fine pitch PQFP packages with gull wing leads is shown in Figure 3.

Materials for Electronics Packaging

There are several different organic and inorganic materials (see Figure 2B) used to package microelectronic devices, including two principal metal alloys for molded plastic packaging: copper-rich alloys and iron-nickel alloy. Iron-nickel has a coefficient of thermal expansion closer of silicon, and better mechanical properties than the copper-based alloys. The disadvantage of iron-nickel is its low thermal conductivity. The growing heat dissipation needs of larger devices have required using copper alloys, accepting their limitation on thermal expansion and mechanical properties.

The metal leadframe influences important processing and performance characteristics such as deformed inner leads during molding, heat dissipation, yield of the trim and form operation, thermomechanical shrinkage mismatch, and mechanical robustness of the leads during attachment to the printed circuit board. Leadframes are formed from punched sheet stock. Those requiring high interconnection density, such as 164-lead packages and above, have to be etched because the inner lead spacing is too small to form with a punching tool. Gold or aluminum wires are used to connect the tips of the leads to the bond pads on the device. The silicon device is attached to the leadframe with a die-attach material: typically a conductive polymer, eutectic solder, or silver-glass composite material. Conductive polymer adhesives are displacing solders for die-attach, because they are cheaper than gold-containing eutectic materials, and are more easily automated.

Polyimides are important packaging materials for interlayer dielectrics, conformal coatings, die-attach materials, and reinforcement tapes for the fragile leads. This class of materials results from the reaction of dianhydrides and diamines to form an intermediate polyamic acid (PAA) that is soluble in polar solvents. PAA is then

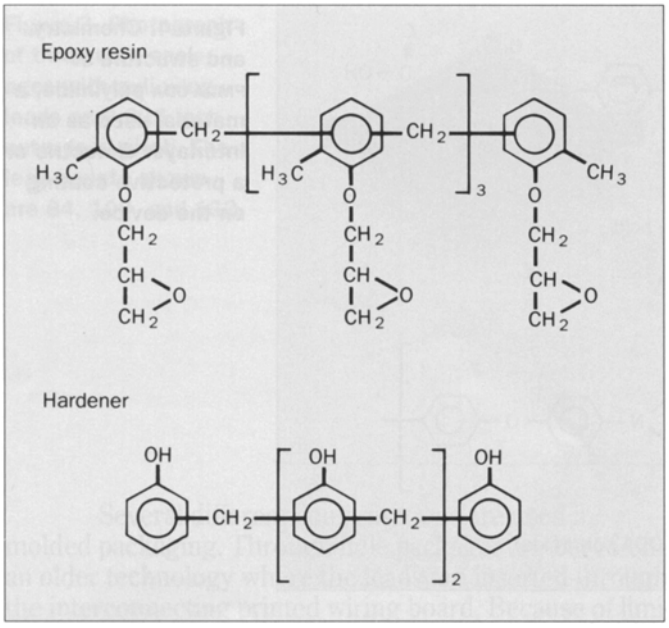

Figure 5. The chemical structure of the novolac epoxy resin and phenol novolac hardener used in most molding compounds for plastic packaging.

applied and baked to complete the imidization reaction, providing the final chemical structure shown in Figure 4.

There are many aromatic diamines and aromatic dianhydrides that can be reacted to form high temperature polymers. Differences in the resulting molecular structures determine the differences in the material's physical properties. Polyimides with excessively rigid polymer backbone structures, because they are too brittle, often are inappropriate for microelectronic applications. New innovations in polyimide materials seek to lower their coefficient of thermal expansion and make them less susceptible to moisture uptake.

Among the most important materials in molded plastic packaging is the thermoset polymer molding compound itself.[1] The molding polymer is converted from low-viscosity fluid to hard plastic during the process. Although they have a softening point, or glass transition temperature, they do not flow after polymerization, even at soldering temperatures, because they have a cross-linked molecular architecture.

Epoxy is the cross-linkable resin for nearly all commercial molding compounds. The formulation consists of a complicated (often proprietary) mixture of epoxy resin, hardener (or curing agent), catalyst, fillers, flame retardants, flexibilizers, coupling agents, mold release agents and colorants. The chemical structures of the novolac epoxy and cresol novolac hardener used in many commercial systems are shown in Figure 5.

Important molding compound properties include low viscosity to prevent damage to the fragile assemblies during molding, rapid cure to provide high productivity, and low thermal shrinkage forces caused by disparities in coefficient of thermal expansion (CTE) among molding compound, leadframe, and silicon die. The thermomechanical shrinkage stresses are proportional to the integral of the molding compound modulus, the difference in the coefficients of thermal expansion, and the temperature excursion as shown below:

$$\sigma = \int E_p \, (\alpha_p - \alpha_s) \, d\, T \qquad (1)$$

New low-stress molding compounds have low CTE and low modulus to minimize the stresses generated; excellent strength to resist the cracking these stresses promote; and good adhesion to die and leadframe to disseminate the stresses over the entire package volume. The molding compound contains about 75 percent by weight inert inorganic filler, e.g., ground silica to lower CTE and increase thermal conductivity. Higher filler loadings achieved through improvements in filler size and size distribution have lowered the CTE while reducing the material viscosity.

Many important innovations have been made in elastomer modifiers for molding compounds to improve their toughness and strength, and lower their modulus. These rubbery materials are incorporated as a second

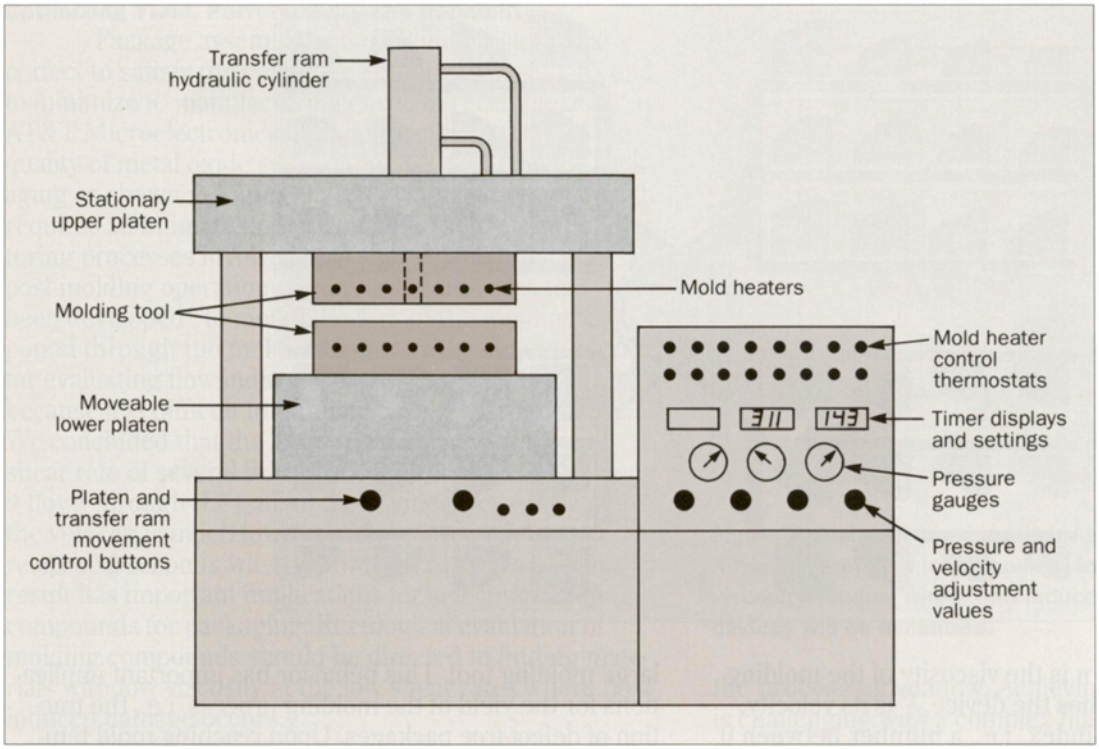

Figure 6. A diagram of the transfer molding machine and molding tool used to manufacture molded plastic packaging.

phase in a dispersed domain morphology. The effectiveness of the elastomer modification depends heavily on the size, size distribution, and interfacial bonding of these domains.[2] Reductions in thermomechanical stress and improvements in toughness have allowed molded plastic packaging to provide high reliability while placing larger silicon devices into smaller volume packages.

Package Molding Process

Nearly all post-molded plastic packages are made by a transfer molding process using thermoset molding compounds (see Figure 6). The molding compound is pre-softened by heating it in a dielectric preheater above its glass transition temperature. It is then placed in a cylindrical cavity in the molding tool. The assembled leadframes have already been loaded on the molding tool either manually or with an automated leadframe loader. The operator starts the transfer by beginning the plunger movement that pushes the molding compound out of the transfer pot and into the mold (see Figure 7). A production molding tool consists of up to several hundred cavities connected by flow channels known as *runners*. The flow generates flow-induced stresses on the fragile IC assemblies that can lead to damage and yield loss. The magnitude of these forces is proportional to the product of the molding compound velocity and viscosity. Viscosity is more important than velocity here, because the molding compound is a shear-thinning fluid:

$$\text{Flow Induced Forces} \propto \eta V^n \qquad (2)$$

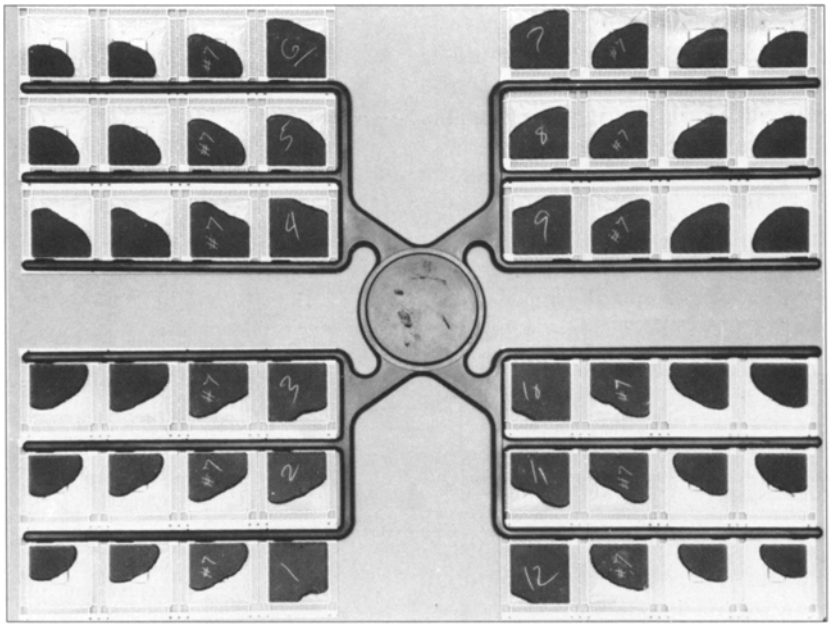

Figure 7. Photograph of an incomplete fill of a production size packaging mold for 40 pin DIPs. Ninety-six devices are encapsulated in a 3-minute molding cycle with this tool.

In this relation, η is the viscosity of the molding compound when it reaches the device, V is its velocity, and n is the power law index, i.e., a number between 0 and 1 that characterizes the extent of shear thinning behavior. Materials that show greater reduction in viscosity with increasing shear rate have an index closer to zero. Molding compounds are moderately shear thinning, and have indices around 0.5. In addition to the shear thinning character, the molding compound viscosity also changes with time and temperature. The molding compound enters the mold at about 100° C, but the mold temperature is 175° C. Thus, the molding compound heats as it flows through the mold. However, because the molding compound is polymerizing as it flows at these high temperatures, the viscosity at constant shear rate and constant temperature will increase with time.

Figure 8 charts the effect of temperature and time on viscosity,[3] showing a computed plot of the viscosity of a single fluid element as it flows in the runner system of a large molding tool. This behavior has important implications for the yield of the molding process, i.e., the fraction of defect-free packages. Upon reaching mold temperature, the viscosity is low. The flow-induced forces are lowest when the molding compound encounters the devices while within this low viscosity window. Precise control can be difficult, however, when using large molding tools such as the one shown in Figure 7 that provide high production rate but cause the largest spread in the times that the molding compound reaches the different cavities of the tool.

After mold filling, the pressure is increased and the molding compound is packed and further polymerized under a higher applied pressure than that used to fill the mold. Packing is important because the material is porous after filling. Therefore, packing compresses both macroscopic and microscopic voids in the molded body, lowers package permeability, and eliminates voids where liquid water could collect and promote corrosion.

Optimizing Yield, Performance, and Reliability

Package assembly and molding must be nearly perfect to satisfy the customer's quality expectations and to minimize IC manufacturing costs. In recent years, AT&T Microelectronics has significantly improved the quality of metal oxide semiconductor (MOS) device packaging as shown in Figure 9. Achieving near-perfect yield requires an intimate understanding of the many manufacturing processes involved in assembly, molding, and post-molding operations. Computer simulation tools have been developed[4] to model the flow of the molding compound through the mold. They provide the parameters for evaluating flow-induced stress (shown in Equation 2) because it is difficult to evaluate them experimentally. We concluded that the molding compound sustains a shear rate of several thousand reciprocal seconds when it flows through the gate of the cavities, yet—because the velocity is much lower at this point—only tens of reciprocal seconds when it flows over the device. This result has important implications for selecting molding compounds for packaging. Rheological evaluation of molding compounds should be directed to finding materials with low viscosity at the low shear rates where flow-induced damage occurs.

The filling profile of the molding tool also affects yield and productivity. In most conventional molding tools, all gates are uniform in geometry, and the flow resistance they offer is equal. Therefore, the resulting filling profile is non-uniform (see Figure 7) because the pressures are higher closer to the transfer pot. The implications of the filling profile can be important in reducing flow induced forces. Uniform filling divides the volumetric flow rate into the mold over the largest number of cavities, thereby lowering the velocity in each cavity and lowering the flow induced force according to Equation 2. More important, however, is the point on the viscosity versus time plot (Figure 8) where the molding compound contacts the devices. Uniform filling clusters the cavity fill times together because all cavities fill simultaneously. This makes it easier to center them within

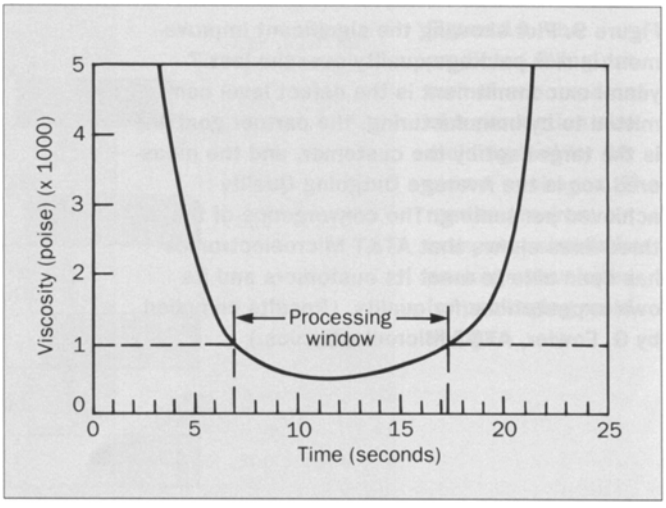

Figure 8. A plot of the viscosity of a single fluid element as it moves through a large molding tool. The plot shows a low viscosity window where flow-induced stresses on the devices will be minimized.

the processing window. Achieving balanced mold filling is challenging with a complex fluid such as the epoxy molding compound whose viscosity changes with time, temperature, and shear rate.

Designing molding tools and selecting materials for specific fill patterns requires sophisticated flow simulation packages that have been developed by AT&T specifically for microelectronics packaging.[4] Figure 10 shows the predicted fill pattern for one quadrant of a production-size molding tool where changes have been made to the runner cross sections and uniform gate sizes to promote more balanced filling.

The reliability of the molded package is critical to product quality. Molded packages provide excellent reliability for most consumer and telecommunications applications. Early work on reliability showed that plastic packages could meet the customer's expectations for AT&T products even when subjected to the harshest

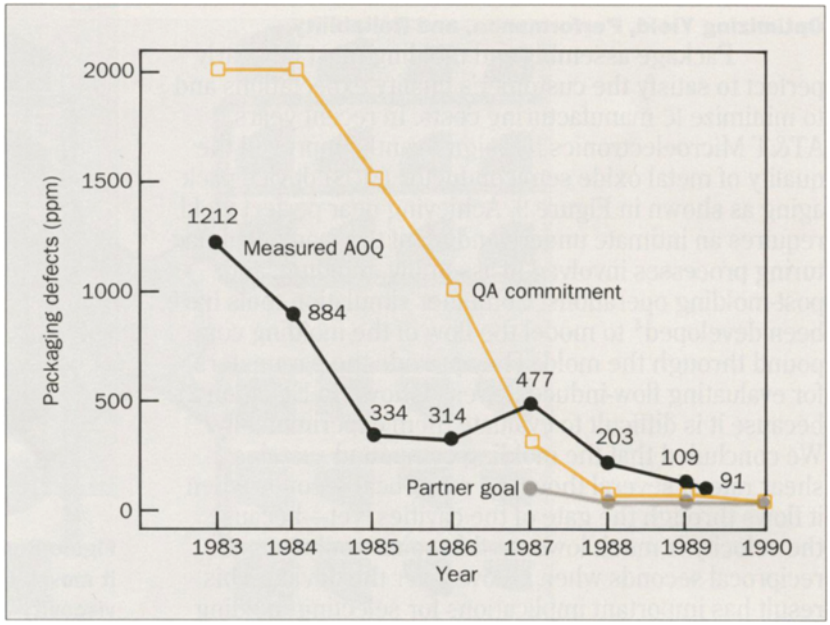

Figure 9. Plot showing the significant improvement in MOS package quality over the last 7 years. QA commitment is the defect level committed to by manufacturing, the partner goal line is the target set by the customer, and the measured AOQ is the Average Outgoing Quality achieved per testing. The convergence of the three lines shows that AT&T Microelectronics has been able to meet its customers and its own expectations for quality. (Results compiled by G. Fowler, AT&T Microelectronics.)

environments. These findings prompted a commitment to design, develop, and manufacture plastic packages for AT&T integrated circuits, with the result that AT&T became a leader in the technology. But maintaining high reliability is a continuing challenge, because the devices continue to grow in size, complexity, and interconnection requirements.

There are several well-defined failure mechanisms associated with plastic packaging and most involve one or more of the following phenomena:

- Corrosion introduced by ionic impurities in the molding compound
- Device cracking introduced by differential thermal shrinkage
- Package cracks induced by thermal shrinkage or vaporization of water during surface mount attachment to the printed wiring board.

The ionic impurities present in the molding compound have been reduced to such a low level in the past decade that this issue is no longer important. Moisture-induced failures during surface mount are currently being addressed through new handling procedures and molding compound improvements.

Thermomechanical stress continues to be an important problem because market pressures promote the drive to put larger pieces of silicon in smaller and smaller packages. Stress cracking of the package or passivation layer can occur if the package design or choice of molding compound is incorrect. One approach to address stress is material selection based on evaluating the mechanical properties of the molding compound. There are large differences in properties among commercial molding compounds, and it is impossible to evaluate them all in reliability trials with live devices. Computational techniques such as finite element analysis (FEA) can be used to predict the performance of materials. FEA is also important in evaluating package designs for minimizing thermomechanical stresses and avoiding stress

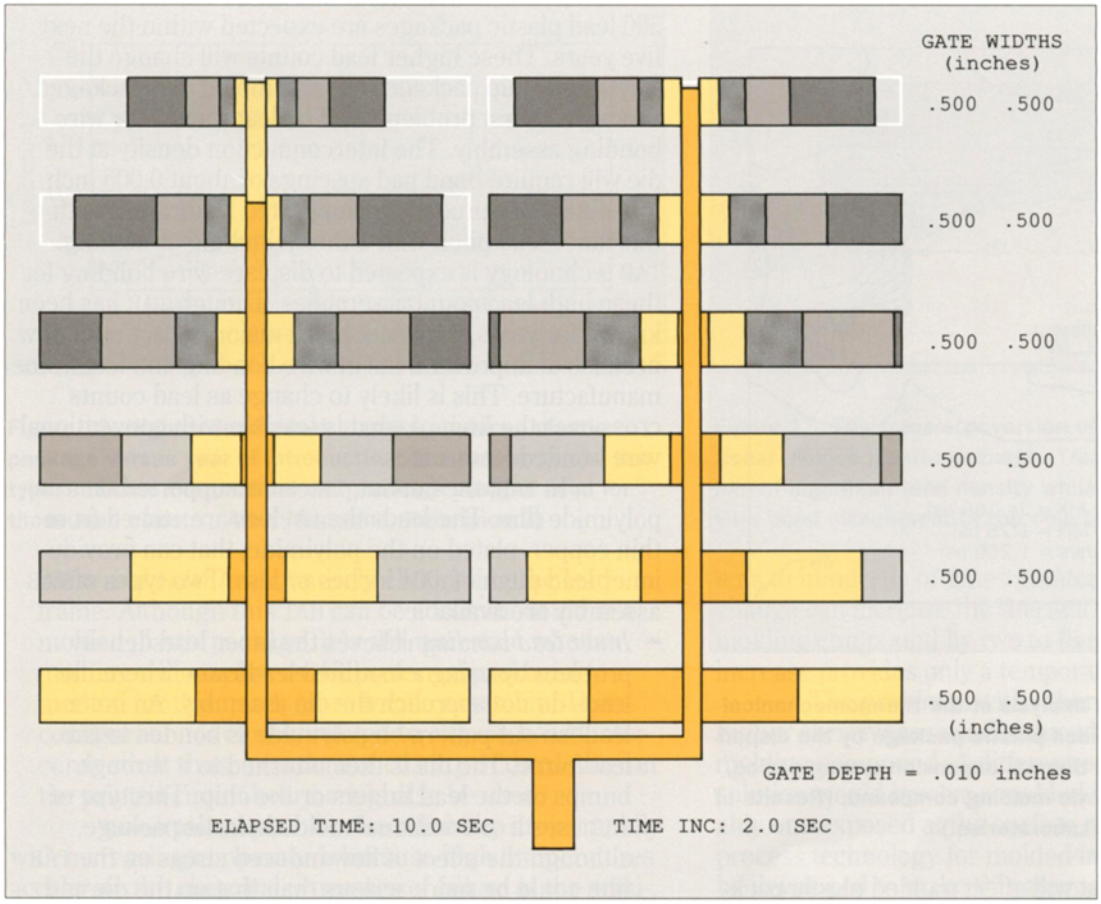

Figure 10. The predicted filling pattern of one quadrant of a production size molding tool for 40 pin DIP packages. The results are from a computer simulation package developed for packaging mold design.

concentration points. An example of applying FEA to predict the stresses in a package is shown in Figure 11. The mechanical property testing discussed previously is also essential to support the FEA evaluation of the design. Confident predictions of stress levels and propensity for failure require complete mechanical property data.

New Trends in Plastic Packaging

Both device and packaging technology are evolving so rapidly that packaging engineers—to predict future needs—must be aware of industry trends. Packaging falls in the middle of the electronic system assembly process; therefore it is influenced by changes in device fabrication technology that precede it, as well as by trends in circuit board assembly operations and system configuration that follow it. Although it had been taken for granted that any device could be packaged without loss of performance, this will change as soon as packaging and interconnection control the rate of evolution of future improvements in system performance. Several of

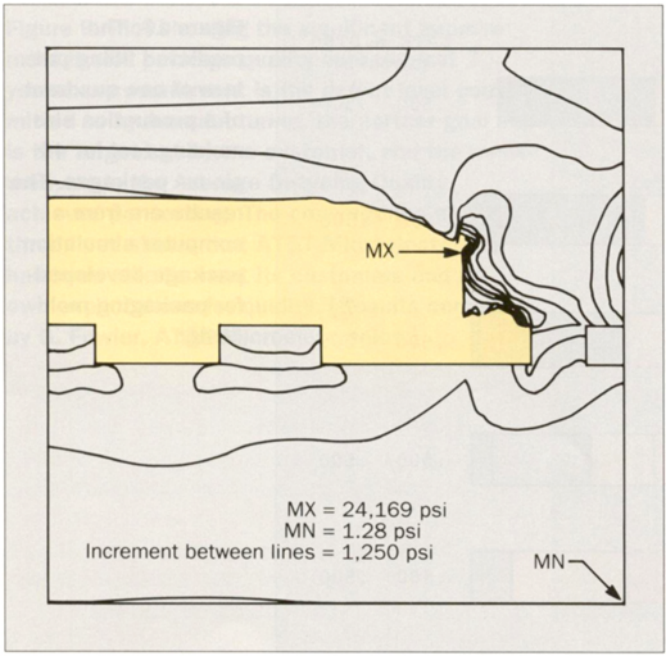

Figure 11. Finite element analysis of the thermomechanical stresses induced in a molded plastic package by the disparities in the coefficients of thermal expansion among device, metal leadframe, and plastic molding compound. (Results of T. M. Sullivan, AT&T Bell Laboratories.)

the important trends that will affect molded plastic packaging are reviewed in the following sections.

Number of I/O. The number of leads a microprocessor needs to communicate with the next level of interconnection depends on the number of logic elements (i.e., transistor gates) it encompasses. Rent's Rule[5] provides an empirical correlation for predicting this number. Reduced device feature sizes and the trend toward larger, more sophisticated devices have resulted in a rapid increase in the number of inputs and outputs (I/O), with some current devices now requiring 200 leads (see Figure 12). This trend is likely to accelerate to the extent that 500 lead plastic packages are expected within the next five years. These higher lead counts will change the way single-chip packages are assembled and packaged. Among the first problems will be leadframes for wire bonding assembly. The interconnection density at the die will require bond pad spacings of about 0.005 inch. It is difficult to produce unsupported leadframes with this inner lead pitch with either punching or etching. TAB technology is expected to displace wire bonding for these high lead count assemblies. Though TAB has been known for years, it has not had a major impact until now because of improvements in wire bonding and leadframe manufacture. This is likely to change as lead counts cross over the limit of what is feasible with conventional wire bonded leadframes.

In TAB, the fan-out pattern is supported on a polyimide film. The leads themselves are etched from thin copper, plated on the polyimide, that can provide inner lead pitch of .004 inches or less. Two types of TAB assembly are available:

- *Inner lead bonding* relieves the inner lead density problem by using a modified leadframe where the leads do not approach the die assembly. An inner lead fan-out pattern on polyimide is bonded to the leadframe. The die is then attached to it through bumps on the lead fingers or the chip. This type of TAB uses a conventional molded plastic package, although the effect of flow-induced stress on the TAB film could be more serious than that on the die and wire assembly. A version of inner lead TAB, known as a translator assembly, was invented by AT&T[6] to realize the benefits of inner lead TAB without waiting for the solder bumping technology needed at the chip bond pads. With *translator*, the bond pads on the chip are wire-bonded to the polyimide-supported leads. These leads are then thermocompression-bonded to the outer leads as in conventional inner lead TAB. The structure is then amenable to conventional molded packaging (see Figure 13).
- The second type of TAB uses *one TAB film for both*

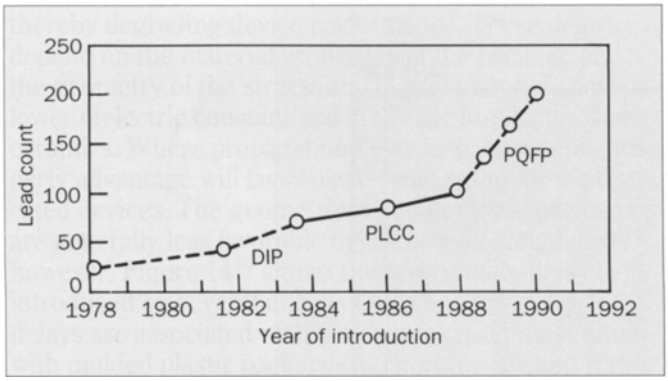

Figure 12. Highest lead count in mass produced plastic package versus year of introduction. The acronyms and line types indicate the predominant package designs used for those lead counts. (After Manzione, Reference 3)

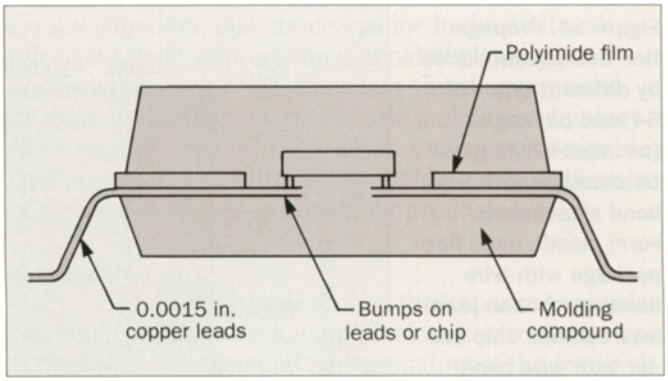

Figure 13. The *translator* version of TAB shown in a conventional molded plastic package. *Translator* relieves the problem of high inner lead density while allowing conventional wire bond attachment of the chip to the fan-out-pattern.

inner and outer leads, entirely eliminating the leadframe. Although this TAB can be accommodated in a molded plastic package, it is still uncertain whether molding will emerge as the preferred packaging method for this much more fragile assembly. This configuration is closely related to chip-on-board interconnection; thus, a conformal coating of the device on the printed circuit board could also be used.

Power Dissipation. Device reliability drops rapidly with increasing temperature because high temperatures accelerate the chemical processes of failure at the semiconductor level. Power dissipation is probably the most urgent issue facing low-cost plastic packaging, because power levels of leading mass-produced products are now at the limit of what can be dissipated through a plastic package while still maintaining acceptable device junction temperatures.[7] Therefore, thermal management has assumed a leading role in preserving plastic packaging.

The thermal conductivity of the molding compound can be increased by switching the inorganic filler from silica to materials such as alumina, silicon carbide, or aluminum nitride that have thermal conductivities tens to hundreds of times greater than silica. This change can increase the thermal conductivity of the molding compound by two to five times. However, this increase provides only a temporary solution.

The problems with other fillers are the sharply higher abrasiveness and reduced flow properties of the molding compound. A different or even complimentary solution would involve a molded-in heat spreader, preferably one exposed at the surface of the package. The process technology for molded-in heat spreaders has to be developed to make this approach feasible. Reliability considerations of introducing a large metal object into the package also have to be addressed.

Multichip Modules. The interconnection densities of the device and printed wiring board are diverging rapidly as feature sizes on the device continue to decrease regularly. However, the interconnect density of conventional printed circuit boards and multilayer boards decrease at a much slower rate[7]. It is becoming more difficult for the package to bridge this widenening gap. The *multichip module* (MCM) is an intermediate interconnection level that fits between the device and the

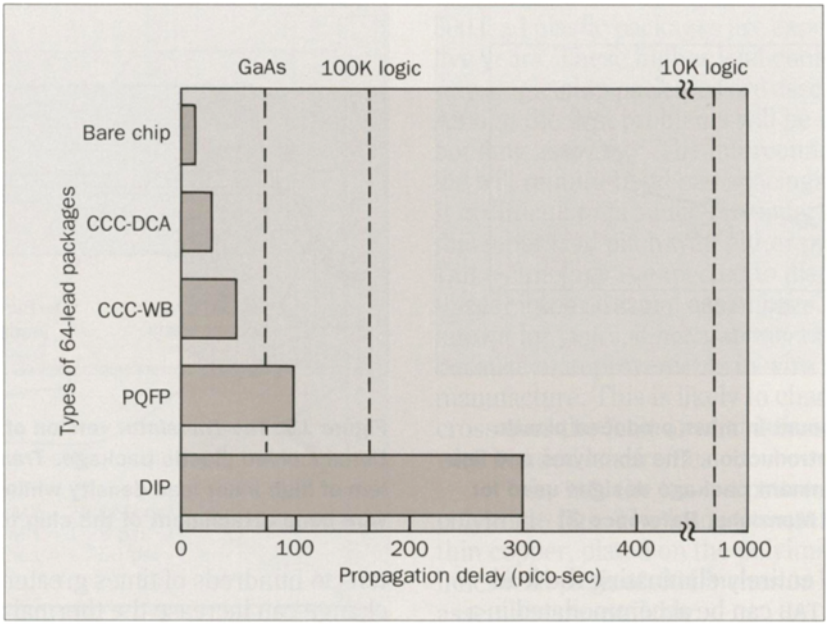

Figure 14. Propagation delays introduced by different types of 64 lead packages. (DIP: dual-in-line plastic package with wire bond attachment, PQFP: plastic quad flat package with wire bonding, CCC-WB: leadless ceramic chip carrier with wire bonding, CCC-DCA: leadless ceramic chip carrier with direct chip interconnection.) (after Sinnadurai, Reference 10)

printed wiring board to bridge this widening gap. A multichip module[8] is a substrate that interconnects several high performance devices through fine line patterns that are produced using the same microlithographic processes used for the chip themselves. Solder bump, TAB, or wire bonding can be used to interconnect the devices to the substrate. Multilayer structures are feasible, but two to three layers are often adequate because of the much higher interconnection density that can be achieved. Silicon, alumina, or printed wiring board are the preferred substrate materials with silicon offering the best CTE match to the silicon devices.

Although current MCMs are expensive devices that often warrant expensive ceramic packages, interest in packaging MCMs in low-cost plastic will undoubtedly develop as the technology matures and competitive cost pressures mount. Plastic packaging of these structures is difficult, however, because the large substrates will allow only a thin edge of molding compound, significantly concentrating the thermomechanically-induced stresses in this region and promoting package cracking. Flowing the molding compound over the large substrate could also create problems in venting the air from the cavity. AT&T has already shown the feasibility of this technology through the development of a molded hybrid integrated circuit (HIC) technology.[9] MCMs differ from HICs in the interconnection density achieved and the sophistication of the devices used; however, the molding and mechanics of the packages are similar. Thermal dissipation from MCMs is likely to be the greatest challenge, because the demands of managing the heat produced from several high-power ICs clustered close together on a silicon substrate will be far greater than any encountered in single chip packaging.

Clock Rates. The propagation delays introduced by the package have been much shorter than the rise times of the devices typically packaged in molded plastic. But in the next several years, developments in miniaturization and faster computation will reduce rise times to within the propagation delays introduced by the package,

thereby degrading device performance. These delays depend on the material properties of the package and the geometry of the structures. Plastic materials have a lower dielectric constant and dielectric loss factor than ceramics. Where propagation delay is an issue, this property advantage will favor plastic packaging for sophisticated devices. The geometries used in plastic packaging are generally less favorable to low propagation delays, however. Figure 14[10] shows the propagation delays introduced by several different package types. Long delays are associated with the designs used most often with molded plastic packages such as the DIP and PLCC packages described earlier. Molded packages typically incorporate high-inductance wire bonds, long fan-out patterns compared to multilayer ceramic structures, and high-inductance leads to the printed circuit board. Therefore, plastic packages will have to evolve toward leadless geometries with direct chip attachment of the device to the fan-out pattern to accommodate high clock rates.

Integrated Optics. Significant growth in optoelectronics is predicted in the near future. As lightwave technology continues to grow, it will continue to move down the interconnection hierarchy toward smaller systems such as personal computers, where it will be found on printed wiring boards and electronic components. This trend will promote rapid growth in the technology of attaching fibers to electronic packages.[11] Optical data links are excellent examples of this type of device.

The implications of optoelectronic packaging are profound because coupling photons into the device requires a precision that is difficult to achieve with conventional mass production methods. This higher precision is possible, but will require extensive development of the materials, machinery, and process parameters. Highly filled thermoset molding compounds have been widely used for precision molding because they polymerize in the mold cavity, eliminating the flow-induced molecular orientation effects that cause deformation. There have been significant advances in the precision of injection molded parts in the last few years as machinery, mold design, and materials have all improved. Liquid crystal polymers, that are crystalline in the melt state, offer new levels of precision in molded plastic parts because these materials show less shrinkage on solidification. Extending low-cost plastic molding technology to packaging optoelectronic devices will provide significant cost reductions that would rapidly promote the use of these components in consumer products.

Summary

This paper has described the important role of materials in plastic packaging of microelectronic devices. A thorough, fundamental understanding of the materials and processes used in packaging has enabled AT&T to become a leader in low cost, highly reliable plastic package technology. Both materials and processes have been refined extensively to provide high yields and high productivity. A confluence of several emerging trends will present significant challenges to the continued use of low cost package molding. These trends include higher lead counts, greater thermal dissipation, higher clock rates and optical interconnection. Packaging for leading-edge products is likely to change rapidly in the coming years in response to these trends. The need to retain low-cost packaging for their economic and assembly advantages assures a place for this technology. Component suppliers who meet these challenges—while retaining the cost, performance and reliability advantages of plastic packages—will enjoy a distinct competitive advantage in the marketplace.

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References

1. N. Kinjo, M. Ogata, K. Nishi and A. Kaneda, "Epoxy Molding Compounds as Encapsulation Materials for Microelectronic Devices," *Speciality Polymers/Polymer Physics*, Ed. Y. K. Gadovsky, *Advances in Polymer Science 88*, Springer-Verlag, Berlin, Germany, 1989, pp. 1-48.

2. Y. Nakamura, H. Tabata, H. Suzuki, K. Iko, M. Okubo and T. Matsumoto, *Journal of Applied Polymer Science*, Vol. 32, 1986, p. 4865.
3. L. T. Manzione, *Plastic Packaging of Microelectronic Devices*, Van Nostrand Reinhold, New York, 1990.
4. L. T. Manzione, J. S. Osinski, G. W. Poelzing, D. L. Crouthamel, W. G. Thierfelder, "A Semi-Empirical Algorithm for Multi-Cavity Mold Balancing," *Polymer Engineering Science*, Vol. 29, No. 11, p. 749.
5. R. L. Russo,"On a Pin Versus Block Relationship for Partitions of Logic Graphs," *IEEE Transactions on Computers*, Vol C.-20, 1971, p. 1467.
6. U.S. Patent No. 4,774,635, issued September 27, 1990. L. A. Greenburg and D. J. Lando. Assigned to AT&T.
7. "Materials for High Density Packaging and Interconnection," Report of the Committee for High Density Electronic Packaging, D. W. McCall, Chairman, National Materials Advisory Board of the National Research Council, National Academy Press, NMAB-449, 1990.
8. C. J. Bartlett, J. M. Segelken, and N. A. Teneketges, "Multi-Chip Packaging Design for VLSI-Based Systems," *Proceedings of the 37th Electronic Components Conference*, May 1987, pp. 518-525; G. E. Blonder, R. A. Gottscho, and K. L. Tai, "Interconnection Processes and Materials," *AT&T Technical Journal*, Vol. 69, No. 6, pp.46-59.
9. R. Biswas, H. Curtis, P. A. Deane, T. F. Marinis, and M. Kaplan, "Molded-Hybrid IC Packages," *IEEE Transactions on Components, Hybrids and Manufacturing Technology*, Vol. 12, No. 4, December 1989, pp. 514-520.
10. N. Sinnadurai, "Advances in Microelectronics Packaging and Interconnection Technologies—Toward a New Generation of Hybrid Microelectronics," *Microelectronics Journal*, Vol. 16, No. 5, 1985, pp. 31-43.
11. D. S. Alles and K. J. Brady, "Packaging Technology for III-V Photonic Devices and Integrated Circuits," *AT&T Technical Journal*, Vol. 68, No. 1, January/February 1989, pp. 83-92.

Biographies (continued)

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