CAE/CAD AT AT&T: AN INTRODUCTION

Jeffrey C. Foster

Jeffrey C. Foster is
head of the Computer-
Aided Design (CAD)
Customer Service
Department at AT&T
Bell Laboratories, Mur-
ray Hill, New Jersey.
His department is
responsible for applica-
tion support of SysCAD
and UNICAD computer-
aided engineering/
computer-aided design
(CAE/CAD) tools. Mr.
Foster received a B.S.
from Brown University,
Providence, Rhode
Island, and an M.S.
from Stevens Institute
of Technology, Hobo-
ken, New Jersey, both
in applied mathemat-
ics. He joined AT&T in
1967.

Computer-aided engineering/computer-aided design
(CAE/CAD) tools have in the past and will in the future
play an important role in the design of AT&T hardware
products. Currently, CAE/CAD tools are being used to
decrease overall product time-to-market and increase
product quality, specifically in the areas of design verifi-
cation and synthesis. This issue of the *AT&T Technical
Journal* contains papers based on the topics presented at
the AT&T CAE/CAD symposium, held in Murray Hill,
New Jersey, on October 18, 1989. This paper discusses
CAE/CAD in general, as well as its past and future roles in
AT&T. It also introduces each paper in this issue and
describes its relationship to advances in the field of
CAE/CAD technology.

Introduction

Computer-aided engineering/computer-aided design—com-
monly known as CAE/CAD—refers to computer tools used in the design
portion of the product realization process. CAE supports the initial logi-
cal design processes, such as capturing design intent or analyzing
design functions. CAD is used to translate the design intent into a physi-
cal implementation, such as the geometric layout of an integrated cir-
cuit (IC) or printed-wiring board (PWB).

CAE/CAD tools encompass various design disciplines—mechan-
ical design of specific hardware parts or assemblies, electrical design
of circuits, or software design (where CAE/CAD is more commonly
referred to as CASE—computer-aided software engineering). The papers
in this issue of the *AT&T Technical Journal* refer to CAE/CAD for electri-
cal design of circuits.

Today, the computer is the major tool used by electrical
designers in executing their job, and the CAE/CAD tools available to
them are a key determinant in how effective these designers can be.
The goals of CAE/CAD development have always been to improve the
quality, time-to-market, and cost of the product being designed.
AT&T's continuing emphasis on these goals and the high-leverage

2

possibilities for CAE/CAD in these areas make effective CAE/CAD even more important as we move into the future.

This issue contains a selection of papers from a recent AT&T CAE/CAD symposium. They were chosen to give a sense of the current topics being addressed in CAE/CAD. In this introductory paper we present an overview of CAE/CAD, discussing the breadth of the field, some history of the efforts, where we are today, and where we expect to be going in the future.

Elements of Electrical CAE/CAD

Electrical CAE/CAD comprises two broad design disciplines—computer-aided engineering and computer-aided design.

CAE focuses on the design of the circuit's *function*. It has the following major components:
- *Design capture.* Various input forms such as truth tables, schematic diagrams, and structural or behavioral hardware description languages are used to capture the logical design intent.
- *Design verification.* Analysis and simulation tools verify that the design captured will in fact execute the function that the designer intends.
- *Design synthesis.* This relatively new field involves the automatic creation of detailed design entities from higher-level descriptions—for example, creating a gate-level description of a design from an RTL (register transfer language) or state-table description, or from a behavioral description of circuit operation.

CAD, on the other hand, focuses on the *physical* design of electrical circuits—that is, the mapping of the functional design intent to interconnected physical entities such as transistors on an integrated circuit, or packaged components on a printed-wiring board. To accomplish this, CAD:
- Assigns logical-circuit elements to physical devices
- Places physical devices on the interconnection media—for example, standard cells on an IC, or dual in-line packages (DIPs) on a PWB.
- Routes paths to complete the circuit interconnection

- Checks the complete physical design to ensure that it correctly creates the functional-design intent and can be manufactured at reasonable costs with high yields.

Two other subfields of CAE/CAD that do not fit easily into the division between CAE and CAD are computer-aided testing (CAT) and technology CAD (TCAD).

CAT tools are used to enhance the creation of manufacturing tests for electrical products at either the device, circuit pack, or system level. CAT does not fit easily into the CAE/CAD breakdown, because the creation of manufacturing tests spans the functional and physical design processes. CAT comprises tools to:
- Add circuitry to the basic circuit being designed that makes it easier to test—so-called design for testability (DFT) functions[1]
- Automatically create tests for circuitry and simulate whether tests will uncover manufacturing defects in the circuitry
- Transform tests into formats that can be used by manufacturing tests.

TCAD tools are used to model the very basic electrical phenomena of circuits and interconnections, as well as the actual physical manufacturing processes used to create circuit elements. These are most notably, but not exclusively, the processes involved in creating semiconductors. By accurately modeling these processes and then deriving "compact models" that can be used in other CAE/CAD design and verification tools, the output of the TCAD tools forms the technological backbone of the CAE/CAD. For example, MOTIS, an AT&T MOS timing simulator, is much more accurate than its competitors and, hence, gives designers a much higher probability of creating designs that are "correct the first time." This is due in large part to the basic timing model in MOTIS, which is drawn directly from TCAD simulations of the AT&T manufacturing and circuit element creation processes.

Evolution

Today, a broad range of CAE/CAD tools are used by all major electronic products manufacturers. In fact,

3

Panel 1. Acronyms and Terms

AGSIM	accelerated good circuit simulator
ASIC	application-specific integrated circuit
CAD	computer-aided design
CAE	computer-aided engineering
DIP	dual in-line package
DFM	design for manufacturability
DFT	design for testability
FPGA	field-programmable gate array
IC	integrated circuit
MARS	microprogrammable accelerator for rapid simulations
MOTIS	metal-oxide semiconductor timing simulator
PLD	programmable logic device
PWB	printed wiring board
RTL	register-transfer language, the earliest high-level language for specifying a design
TCAD	technology computer-aided design

4

CAE/CAD tools represent well over a billion dollar a year business in the commercial marketplace. Much of their broadening use in the commercial market has occurred over the last ten years, although the field has been developing for almost thirty years. Most early work in the CAE/CAD field was developed by large electronics manufacturers—such as AT&T, IBM, RCA, and Siemens— principally for internal use. At the time, only large firms could afford the technological investment and computing hardware necessary.

Much of the early CAE/CAD work predated the integrated circuit and focused either on the physical design of circuit packs with discrete components or the design of discrete wiring for large frames of equipment. It concentrated on passively capturing and plotting physical data (for example, digitizing hand-drawn PWB layouts) or on managing large files of discrete wiring data.

The 1970s introduced the minicomputer and, with it, widespread capabilities for interactive graphics,

which were applied to both PWBs and the new IC market. The initial systems of this era were not much more than slightly interactive digitizers. As such, significant manual effort was still required to check the design intent, normally in a paper schematic, against the PWB or IC layout.

PWB CAD systems quickly evolved that were capable of storing information about design intent, comparing it to the design submitted, and analyzing it for violations during design. In this way, a "correct-by-construction" mode became possible, at least in terms of electrical connectivity. Because of its greater complexity both in the structure of design intent and the geometries needed to realize it, IC design could not operate in the same correct-by-construction mode at that time. Instead, it developed sophisticated capabilities in design-rule checking to ensure that the physical design correctly embodied the logical intent and did not violate tolerance requirements of the IC manufacturing process.

Owing to the high cost of computers, most CAE/CAD work concentrated on CAD. Dedicated groups that could afford dedicated computer resources used CAD for physical design tasks. With the advent of workstations in the 1980s, however, computational power and powerful interactive graphics were made available to the individual engineer. The focus started to switch to CAE, which could create tools to support the individual engineer's circuit design functions.

Capturing schematics was the key element in the initial work, most importantly to feed the correct-by-construction layout tools or design-rule checkers. Very quickly after that, however, significant effort turned to design-verification tools. In particular, emphasis was placed on developing simulation tools for the IC environment, where no viable breadboarding (i.e., building a prototype from discrete components) or lab debugging techniques existed to reduce the number of iterations needed for a successful design. These efforts in design verification were very successful, with initial success rates for IC design rising significantly.

Current Efforts

In the mid-1980s AT&T initiated CAE/CAD efforts with three major objectives: system-level CAE, the integration of CAE/CAD into a total computer integrated manufacture (CIM) environment, and the integration of commercial tools into the AT&T CAE/CAD environment.

In system-level CAE, an integrated CAE environment creates the functional design of an entire system, including the device, board, and system level. Basically, some of the design techniques developed and successfully applied at the device level are applied at the system level, in particular to the simultaneous design of application-specific integrated circuits (ASICs) and boards. To do this, effort has focused on two areas:

- *System-level design verification*—The concept of using simulation and analysis tools to debug a design before it is actually committed to hardware. A key part of this is not just simulating an ASIC by itself, but simulating it in its eventual board environment *before* the device has been created. These steps significantly increase the chances that the ASIC and the board will be right the first time. This technique is proving effective, with right-the-first-time ASICs rising from 50 to 90 percent for projects that used system simulation. The board-level debugging intervals have been dropping dramatically, in one case from an estimated ten months to one month.
- *Synthesis*—The idea of specifying the properties that you want a device to have (e.g., the size of the memory and the number of bytes per word), rather than specifying the gates or transistors it will contain. Using a high-level language, you can then compile the specification for application in various technologies. The analogy to a compiler in software development is very apt, both in terms of the productivity gains and its ease of use. With today's widening use of programmable devices such as programmable logic devices (PLD) and field-programmable gate arrays (FPGAs), along with the standard options of gate arrays or standard cell devices, the importance of having high-

productivity design-capture techniques such as synthesis becomes significant. These techniques will have even more applicability as timing optimization continues to be incorporated.

Incorporating CAE/CAD into a total CIM environment increases the opportunity to minimize both the manufacturing ramp-up interval and the cost in the design environment. For example, in the 1970s the specification of agreed-upon design data formats for manufacturing PWBs reduced the interval between receiving data and beginning manufacture from weeks to hours. The current thrust is motivated by the desire to achieve the same goals for the more complex task of the assembly factory. To meet these goals, we are concentrating our efforts in the areas of:

- *Electronic design-data transfer*—This effort has focused on the specification of agreed-upon design data formats (for example, board description data, stock lists, common component libraries, test data, etc.) and electronic transfer mechanisms. By using these tools, manufacturing information systems can quickly receive and process design data.
- *Design for manufacturability (DFM)*—DFM[2] has emphasized the development of electronic design-rule specifications, audits, and communications mechanisms. As a result, manufacturing considerations can be incorporated into the initial design, rather than being identified and repaired in the factory.
- *Design for testability*[1]—DFT, a special case of DFM, ensures that designs are testable in the manufacturing environment. It typically uses audits and automatic circuit enhancements extensively to improve testability.

The third major objective in AT&T CAD/CAE is the effective integration of commercial tools. Early CAE/CAD tools were created by large companies such as AT&T and IBM for their own use. Their internal CAE/CAD groups of necessity became "full-line suppliers." Today, however, healthy commercial sources of CAE/CAD exist, so it no longer makes either financial or technical

5

sense to continue the role of a full-line supplier.

Developing an appropriate functional and structural plan for such integration has not been easy. It has raised many questions, among them:

- In which key technical areas should we maintain leadership to support our underlying physical technology efforts? For example, losing expertise in certain aspects of IC CAD would severely damage our ability to enhance our basic IC technology.
- In which key areas should we maintain some control to support AT&T's vertical integration? Our factory interfaces for electronic design transfer are a strategic asset that we need to maintain.
- Which functional areas in the design process should we emphasize to give the AT&T designer a technical advantage, both today and in the future? Objective analysis of our major strengths, including those in research, are helping us answer this question.
- How do we discontinue our efforts in certain areas in such a way that the basis of customer processes, data, and expertise in those areas is not disrupted? There are literally billions of bytes of data and hundreds of staff years of training invested in the current tools. Managing that investment for maximum return will not be an easy task.
- What is the most effective way to integrate commercial tools, both for ease of use and cost of integration? Numerous competing methods exist: using a commercial tool as a base, using our tools as the base, using the newly evolving data transmittal and framework standards, or using vendor framework standards. There is no clear winner at this time.

Now that we understand the questions, we are making progress to resolve them as we continue to acquire more tools from our vendors.

Future Directions

To understand the future directions for CAE/CAD, we must first understand the basic forces that drive customers. Some of them—product quality, product cost, designer productivity, and support of evolving device and interconnection technologies—remain constant and crucial. Others—in particular, product time-to-market—are becoming even more important. Product introduction intervals have been cut in half in recent years; nevertheless, they need to be cut again in half or to a third to remain competitive. AT&T's new vision of its business brings other forces into play as well. We must optimize our efforts in CAE/CAD in order to take advantage of the opportunities available in global design and manufacture.

To support these driving forces, we believe the key technical efforts in the next five years will be in the following areas:

- *Development of design frameworks and standards*— "Framework" is a relatively recent term that denotes the structure (databases, user interfaces, process management, file management, etc.) into which CAE/CAD functions fit. The concept of a framework is an excellent one but is still relatively immature. AT&T is well positioned, both technically and in the correct standards bodies, to make a strong contribution in this area.
- *High-speed design*—As designs get faster, electrical effects that have been ignored in the past, or at least handled only at the device level, will become important at the board level and higher. We will be able to take advantage of the strong technical expertise we have developed at the device level to deliver solutions for the board designer.
- *Synthesis*—Today's efforts in synthesis are only the beginning of this technology. New efforts in optimization and the incorporation of timing constraints and testability will broaden the use of this technology. Designers are constantly making tradeoffs between time and cost. Optimizing a lower-cost design increases the time-to-market, whereas designing a higher cost, but readily available, product using off-the-shelf components increases the product cost. The ability to synthesize and resynthesize in different technologies will allow product developers flexibility in time-to-market versus product cost. It will also enable them to change

6

technologies easily as the product matures.

- *Simulation*—We have only begun to harvest the benefits of simulation and other design-verification techniques. There are two obvious extensions with very high payoffs for the future. We will be able to specify designs with high-level functional models so that distributed designs (most specifically, globally distributed design) can be integrated logically long before physical integration is possible. We will also be able to debug embedded software on highly observable, controllable simulation models rather than with in-circuit emulators.

- *Design for testability*—Current DFT techniques for ICs are becoming generally available and easier to use, and the payoff for similar techniques at the board and system level is at least as high. Standards such as Boundary Scan (a low-cost method of determining whether all PWB connections have been made) appear to be able to return significant capital and labor savings in manufacture, and perhaps also in field installation and repair.

- *Architectural tools*—Initial decisions about product architecture have by far the greatest effect on overall product cost and quality. Yet in the past, few computer tools were available to help in the decision process. Continuing efforts in research, such as partitioning, protocol evaluation and validation, and throughput analysis are addressing these issues, however, and bringing these ideas to production will be a major goal in the coming years.

In This Issue

The papers presented in this issue of the *AT&T Technical Journal* describe CAE/CAD tools that are improving design verification and synthesis of electronic designs for circuits.

Several of the papers describe design-verification tools. M. S. Toth describes `makcal`, a program that helps a designer write a program to control an analog circuit simulator. Design verification of large Very Large-Scale

Integrated (VLSI) circuits accounts for a sizable part of design time. Simulators verify a design at various levels of abstraction. A fast, accurate simulator enables the designer to introduce a higher-quality product into the marketplace earlier than otherwise possible. In their paper, P. Agrawal, C. H. Hao, and M. Remillard describe a logic simulator implemented using the microprogrammable accelerator for rapid simulations (MARS) multicomputer. The accelerated good circuit simulator (AGSIM) logic simulator has been integrated into the production CAD system at AT&T Bell Laboratories. This paper presents the relevant features of the MARS architecture, and the details of the AGSIM logic simulator.

Advances in simulation have contributed to the successful design of large electronic systems. J. Bierbauer et al. explore how system simulation using MIDAS enables new designs to be brought to the marketplace in less time, at lower cost, and with higher operating speeds and better reliability.

Multichip modules, wafer-scale integration, and three-dimensional connections are the latest solutions to building faster computers. Unfortunately, these new technologies will compound the problems in VLSI testing. Without a systematic approach, testing even a single VLSI chip could be difficult. In her paper, E. Wu describes PEST (Pseudo-Exhaustive Self-Test), a Built-In Self-Test (BIST) design methodology that addresses the VLSI testing problem. In their paper, K.-T. Cheng and V. D. Agrawal present three approaches to designing sequential machines that are capable of generating tests. In the first approach, they develop a partial scan method in which scan flip-flops (one-bit memories) are selected to break up the cyclic structure of the sequential circuit. In the second approach, a novel state assignment method results in reduced feedback or pipeline-like structure. The third approach, also applicable to finite-state machines, embeds a suitably designed test machine in the given specification before synthesis.

One paper in this issue describes tools that provide integrated design environments. An incremental

7

CAD library has been developed that provides run-time facilities to link, unlink, execute, and list functions. At the heart of the library is an incremental loader that helps designers and users customize their basic tool for their design environment. Developers of this enabling technology are J. L. Schmidt, T. J. Kowalski, and D. S. Smull, who relate how four CAD tools have benefited from using a library of functions and designs for simulating C-language models; modifying and enhancing graphical-user interfaces; extending command languages; and rapidly testing new functionality.

J. O. Coplien's paper describes a system-development environment that permits users to specify, prototype, simulate, develop, and document a complex digital system. ISHMAEL can manage the simultaneous evolution of a system's software and hardware. Users of ISHMAEL can develop faithful models of system performance that simulate the interaction of hardware and software at any level of detail. They can iterate hardware and software designs during a simulation, which permits realistic evaluation of design tradeoffs and implementation alternatives early in a system's life cycle and, thus, reduces system costs. ISHMAEL's integrated, graphical interface provides several views of the application being developed: a high-level or a detailed (schematic) hardware view, and the application-user's view.

The remaining paper in this issue describes CAE/CAD tools that improve synthesis. P. A. Subrahmanyam discusses specification and automated synthesis techniques for designing systems with interacting asynchronous and synchronous components. These specification and synthesis techniques allow individual process implementation to be either synchronous, asynchronous, or combinational. A designer can improve design quality by synergistically exploiting the advantages of both the synchronous and asynchronous design styles in a system, and by supporting experimentation with tradeoffs in granularity and implementation strategies.

Summary

CAE/CAD tools continue to play an important role in the design of AT&T hardware products. Currently, CAE/CAD tools are improving design verification and synthesis. Future efforts in these and other areas will help to decrease the time it takes to bring a product to market while increasing product quality.

References

1. D. R. Aadsen, M. N. Scholz, and Y. Zorian, "Automated BIST for Regular Structures Embedded in ASIC Devices," *AT&T Technical Journal*, Vol. 69, No. 3, May/June 1990, pp. 97-109.
2. L. Liu, W. A. Nazaret, and R. G. Beale, "Computer-Aided Design for Quality (CADQ)," *AT&T Technical Journal*, Vol. 69, No. 3, May/June 1990, pp. 46-60.

8