RADIATION-HARDENED MICROELECTRONICS

James L. Jorgensen and David S. Yaney

James L. Jorgensen *works for Sandia National Laboratories in Albuquerque, New Mexico, and* ***David S. Yaney*** *is with AT&T Bell Laboratories in Allentown, Pennsylvania. Mr. Jorgensen is Division Supervisor of multichip and custom products in the Microelectronics Products Department. He is responsible for multichip modules and integrated circuit products that contain custom complementary-metal-oxide semiconductors. He received a B.S. and an M.S. from the University of Nebraska, Lincoln, and a Ph.D. from the University of New Mexico, Albuquerque, all in electrical engineering. He joined Sandia in 1966, and in 1984, transferred to Signetics Corporation. He returned to Sandia in 1988. Mr. Yaney is Head of the Memory Technology Development Department, where he is responsible for technology*
(continued on page 36)

Many nuclear power, defense, and space applications require radiation-hardened integrated circuits. In 1986, Sandia's expertise in microelectronics radiation hardening was combined with AT&T's 1.25-micrometer (μm) complementary-metal-oxide semiconductor (CMOS) process to develop a new generation of digital designs. These include a 32-bit microprocessor and a 256-kilobit static random access memory (SRAM). This effort is now complete; the new process is running at AT&T's Allentown, Pennsylvania, MOS V production facility, and the technology has been transferred to Sandia's Microelectronics Development Laboratory (MDL) in Albuquerque, New Mexico. By joining their resources and expertise, Sandia and AT&T developed this process at a fraction of what it would have cost if either had attempted it alone.

Introduction

Many defense and space systems require electronics that can operate in a high-radiation environment. The radiation may emanate from many sources, including nuclear weapon detonation, the Van Allen belts (which affect earth-orbiting satellites), or deep-space cosmic rays. Most devices manufactured using commercially available CMOS processes can only withstand from one to ten thousand rads (Si) of ionizing radiation. (A rad is the deposition of 100 ergs/gram, i.e., energy/unit mass, in the material of interest, here silicon.) Devices produced using the radiation-hardened process we describe can withstand more than one million rads (Si). Such radiation-hardened devices could extend the useful lifetime of an earth-orbiting satellite by three orders of magnitude beyond that of unhardened devices.

In this paper, we describe the major types of radiation and review the goals and milestones of this joint development. We also examine the differences in the process of creating a radiation-hardened and a conventional CMOS device, describe some characteristics of radiation-hardened devices, and offer conclusions.

Panel 1. Abbreviations, Acronyms, and Terms

BPTEOS — boron phosphorus tetraethylorthosilicon
CMOS — complementary-metal-oxide semiconductor
CMOS V — double-polysilicon, double-metal, complementary-metal-oxide semiconductor process
DDL — Device Development Laboratory
erg — the unit of work and of energy in the centimeter-gram-second systems. The erg is 10^{-7} joule.
IC — integrated circuit
LET — linear energy transfer
MDL — Microelectronics Development Laboratory
MeV — million electron volts
MOS — metal-oxide semiconductor
MOS V — Production Wafer Fab
PETEOS — plasma-enhanced tetraethylorthosilicon
rad — deposition of 100 ergs/gram in the material of interest
SEU — single-event upset
Si — silicon
SRAM — static random access memory
TEOS — tetraethylorthosilicon

Radiation Effects Definitions

There are four major phenomena to be considered in radiation-hardening a modern CMOS integrated circuit (IC): total dose, transient dose, latch-up, and single-event upset (SEU).

Total dose describes the total amount of radiation a part receives, measured in rads (Si). The total dose primarily affects the gate and field oxides of a CMOS-produced IC. In a metal-oxide semiconductor (MOS) transistor, the gate oxide dielectric separates the control gate, usually made of polycrystalline silicon (polysilicon), from the conduction channel in the silicon substrate. The field oxide, referred to as a field transistor, provides electrical isolation between switching transistors. Ionizing radiation can create both bulk oxide and surface anomalies that can reduce the transistor gain and shift the threshold voltage of switching transistors and field transistors. Total dose accumulation will cause a device to fail if:

- The normal switching transistor threshold shifts far enough to cause a circuit malfunction
- The device fails to operate at the required frequency
- The field transistor no longer provides the required electrical isolation.

Transient dose effects occur whenever the ionizing radiation dose rate from gamma and X-rays becomes high enough to cause a temporary circuit malfunction. Usually, this effect is detected first in binary storage circuits (e.g., memory cells, latches) and, in turn, defines the logic upset capability of the process. (*Logic upset* results when radiation reverses the intended state of an internal circuit node.)

Latch-up[1] is a concern in a CMOS process because both NPN and PNP parasitic bipolar transistors are present. (NPN and PNP refer to the two basic types of bipolar transistors. In this context, they are called parasitic because they arise unintentionally from the structure.) These devices are normally biased off (i.e., they conduct zero current), but transient radiation or cosmic rays may generate enough electrons and other free carriers to activate them. If these bipolar devices become active, they may trigger a latching action that generates high, sustained current flow through the device. This anomaly can only be eliminated by turning off power to the device, but the IC may be permanently damaged as a result of the excess current flow.

SEU occurs when a single cosmic ray or particle impinges on a device. The particle generates free charges as it passes through the semiconductor, and those charges are collected by junctions. The net effect is that the circuit is perturbed by an asynchronous noise pulse and may lose data. SEU has become an increasing concern as ICs begin to use increasingly smaller device geometries. At the 1.25-μm level, transistor areas and

Panel 2. Milestones of the Radiation-Hardened Process

3/86	Joint development project authorized
12/86	First test chip lot completed at AT&T Device Development Laboratory (DDL)
3/87	Design goals for 64-kbit/256-kbit SRAMs defined
5/88	First 64-kbit SRAM lot, functional die produced at DDL
7/88	First SA3300 microprocessor lot, functional die produced at DDL
10/88	Began transferring process to Sandia Microelectronics Developement Laboratory (MDL)
5/89	First 64-kbit SRAM lot manufactured at AT&T Production Fabrication (MOS V)
10/89	First 64-kbit SRAM lot manufactured at MDL
9/90	Technical transfer to MDL completed

nodal capacitances are so small that even a single cosmic particle can generate enough local charge to upset the logic state of a binary storage element. Although this damage is not permanent, data stored in these digital memory elements may be corrupted.

Program Goals and Milestones

The goal of this joint program was to develop a radiation-hardened 1.25-μm CMOS technology that could be used in a new generation of digital designs. Panel 2 lists the program's major milestones.

At the beginning of the project, we created a group of test structures and small circuits that could be used for process development. As soon as we established basic process modules, we designed a useful product — a 64-kbit SRAM. We also instituted methods for measuring acceptable fabrication yields. Our final goal was to transfer this technology back to the Sandia MDL and manufacture these devices. Table I shows the radiation-hardening levels achieved in this process.

The Radiation-Hardened Process. Changes were made in the AT&T baseline process to address each of the radiation concerns described earlier. To improve the total dose, we changed both the gate and field oxides. Although we altered the environment in which the gate oxide was grown, the resulting thickness remained the same.

We also changed the field oxide process. The original AT&T commercial process that created the field oxide used a thermally grown oxide. In this process, the

Table I. Levels for a Radiation-Hardened Process

Major Phenomena	Radiation Levels Achieved
Total dose	>1E6 rads (Si)
Logic upset	>1E9 rads (Si)/second
SEU	LET* threshold >20 MeV-cm2/mg (without resistors) LET threshold >100 MeV cm^2/mg (with resistors)
Latch-up	No SEU or transient dose induced latch-up

*LET = linear energy transfer to a material per unit mass by a cosmic particle. LET = $1/dE/dx$ or energy deposited per unit path length of the particle.

radiation-hardened field oxide is deposited on the wafer instead of being grown thermally. The larger steps and steeper edges of this field oxide changed the topography of the underlying field structures relative to the thermally grown field. As a result, later processing of the metal interconnect layers became more difficult.

To prevent latch-up and maximize transient upset levels, we added a thin epitaxial layer on a heavily doped substrate and then modified the circuit layout design rules. The heavily doped substrate was used to degrade the latch-up bipolar structures, thereby eliminating the effect. This, in turn, raised the threshold at which logic upsets occur. In a high transient radiation environment, ionizing radiation can generate several amperes of photocurrent in an IC measuring a quarter of an inch on one side. Modifying the layout rules lets the electrical contacts dissipate the photocurrent more effectively, thereby increasing resistance to logic upsets. The thin epitaxial layer also reduces the amount of photocurrent generated.

To improve SEU performance, we added a resistor in the feedback path of binary circuit elements. With nodal capacitances, this resistor slows the feedback response after a cosmic ray strike. Transistors can then be restored to normal node voltages before the binary

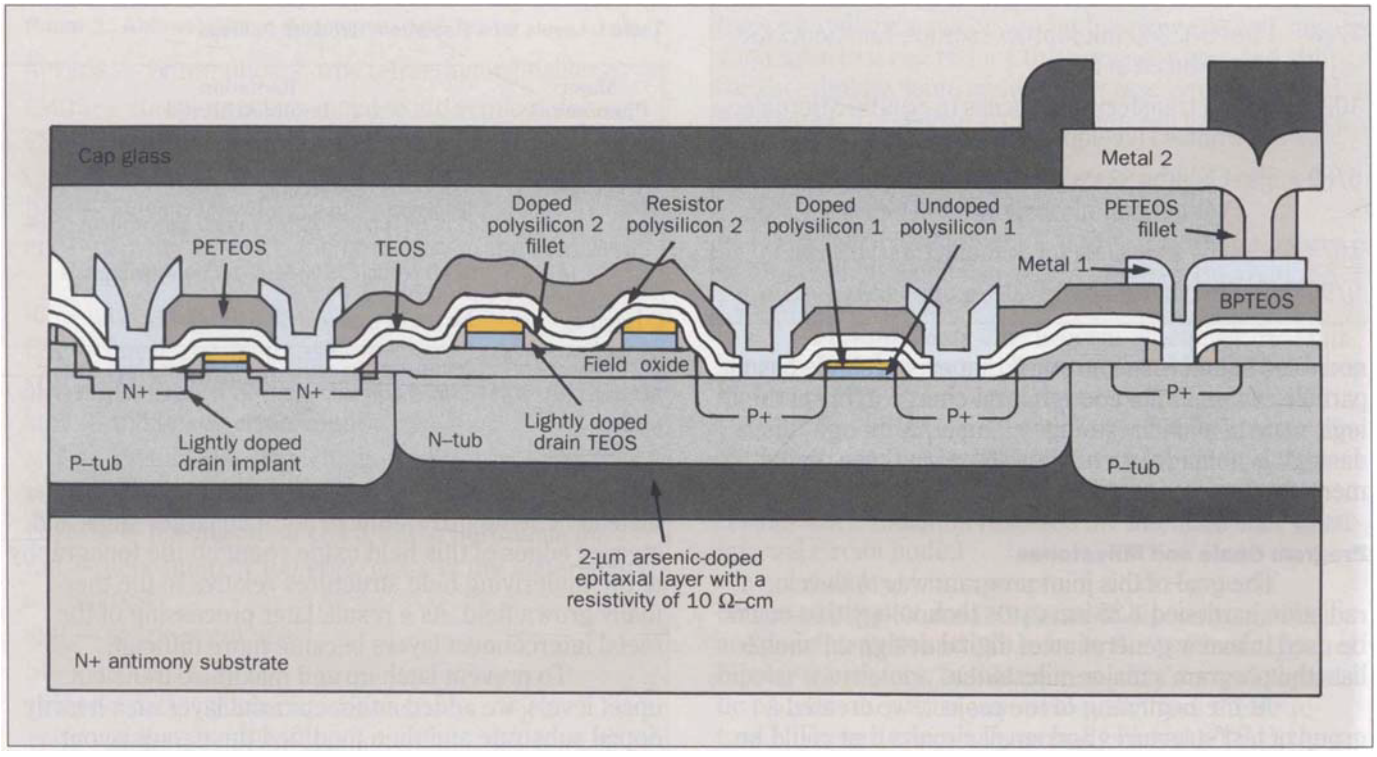
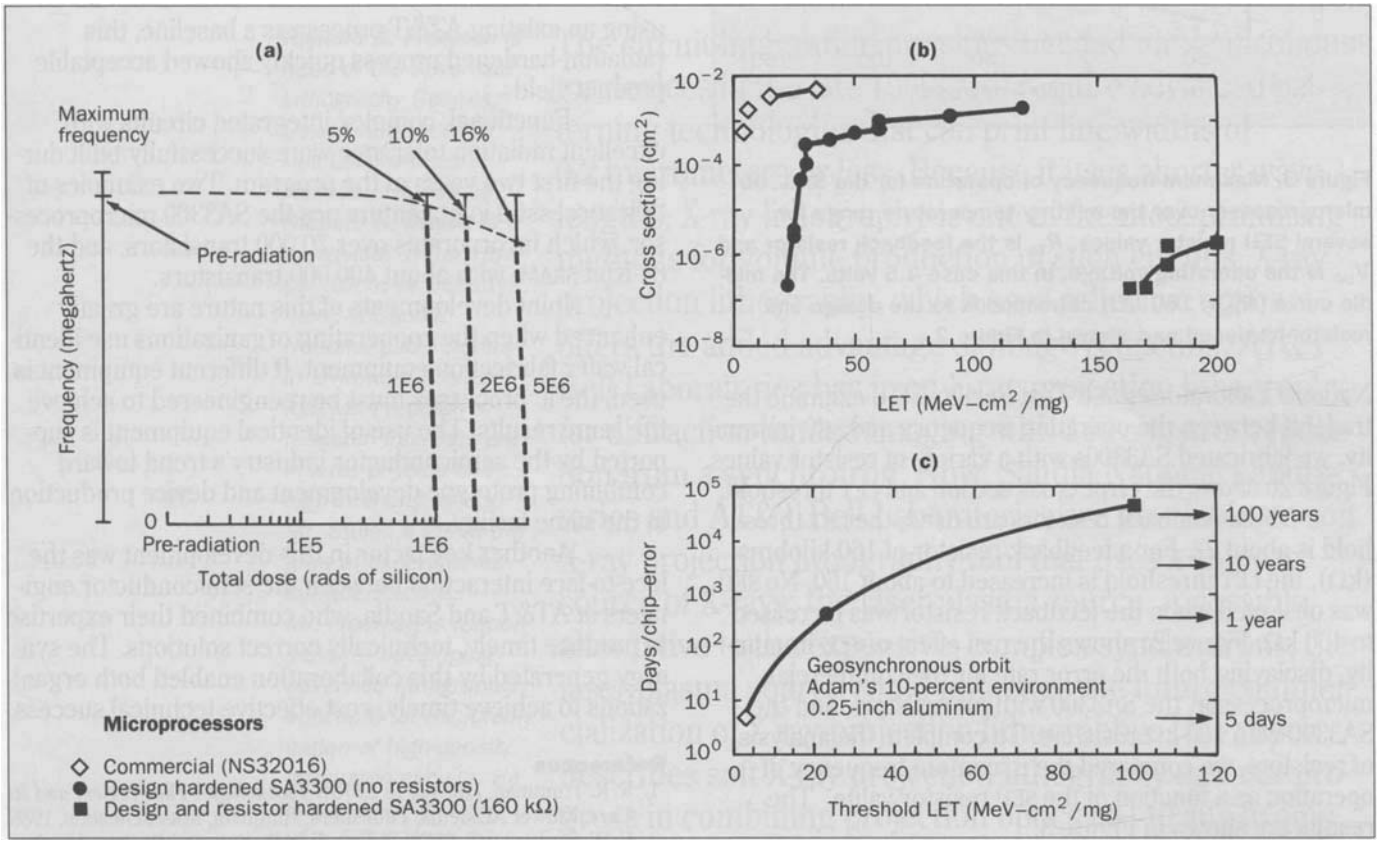


Figure 1. Cross section of the double-polysilicon, double-metal process for CMOS V.

circuit is inadvertently upset to the opposite state. During this process, we added a second polysilicon layer to the device, along with an additional contact layer to connect the resistors. As we increased the size of the resistor, the circuit became slower during normal operation, but more immune to SEU. Circuit designers must balance these constraints to achieve both acceptable circuit speed and SEU immunity.

We also changed the baseline process in minor ways. For example, free hydrogen is known to affect the radiation stability of oxides. To minimize the free hydrogen present, we modified the deposition process for the top passivation glass. Figure 1 shows a cross section of the resulting double-polysilicon, double-metal process, called CMOS V at Sandia.

Hardened Device Characteristics. Using the CMOS V process, Sandia has designed a family of microcontroller, microprocessor, and peripheral devices. The SA3300 microprocessor is a radiation-hardened version of the NS32C016 16-bit microprocessor, produced under license from National Semiconductor. AT&T produced the SA3300, and Sandia has delivered devices to such programs as the California Institute of Technology's Mars Observer Camera project and the International Solar Terrestrial Physics project at the National Aeronautics and Space Administration's Goddard Space Flight Center in Greenbelt, Maryland. Data collected from the



performance of the SA3300 represents what can be achieved using the CMOS V process.

As total dose accumulates in a device, there is a gradual reduction in the maximum operating frequency. Figure 2a shows the maximum operating frequency of the SA3300 as a function of accumulated dose. The device fails when the operating frequency drops below that required for normal system performance. The SA3300 has a measured logic upset threshold of 1E9 rads (Si)/second. Latch-up was not observed within an effective LET of 200 MeV-cm^2/mg.[2]

SEU testing was performed at the Brookhaven

Figure 2. (a) Degradation of the SA3300 microprocessor maximum operating frequency as a function of total dose accumulation. Typical preradiation operating frequencies are 20 to 30 megahertz. (b) SEU response of the Sandia SA3300 and the National Semiconductor NS32016 microprocessors. Note the major decrease in cross section of the SA3300 with resistors compared to the same part without resistors and to the commercial part (NS32016). (The NS32016 data was published by D. K. Nichols, et al., in Jet Propulsion Labs Publication 88–17.) (c) SEU error rate for a typical earth orbit for the Sandia SA3300 and the National Semiconductor NS32016 microprocessors.

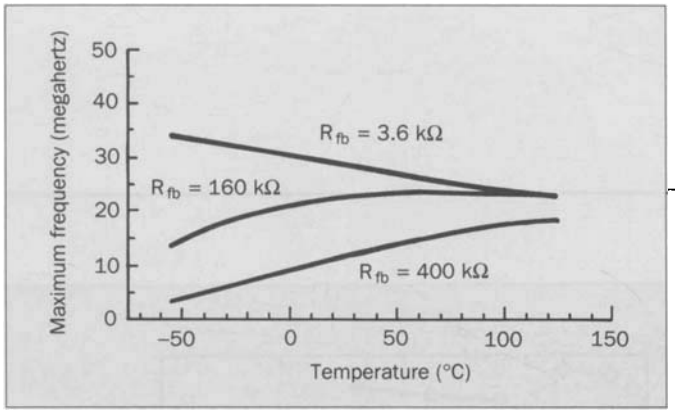


Figure 3. Maximum frequency of operation for the SA3300 microprocessor over the military temperature range for several SEU resistor values. R_{fb} is the feedback resistor and V_{DD} is the operating voltage, in this case 4.5 volts. The middle curve (R_{fb} = 160 kΩ) corresponds to the design and resistor-hardened part shown in Figure 2.

National Laboratories SEU Test Facility.[2] To examine the tradeoff between the operating frequency and SEU immunity, we fabricated SA3300s with a variety of resistor values. Figure 2b shows the error cross section and LET threshold.

If no feedback resistors are used, the LET threshold is about 22. For a feedback resistor of 160 kilohms (kΩ), the LET threshold is increased to about 160. No SEU was observed when the feedback resistor was increased to 400 kΩ. Figure 2c shows the real effect of SEU immunity, displaying both the error rate for the commercial microprocessor, the SA3300 without resistors, and the SA3300 with 160-kΩ resistors. To complete the analysis of resistors, we compared the maximum frequency of operation as a function of the SEU resistor value. The results are shown in Figure 3.

A comparison of the data in Figures 2c and 3 reveals that the SA3300s with 160-kΩ resistors meet a minimum system operating frequency of 10 megahertz (MHz) and exhibit an error rate of less than one error in 100 years.

Conclusions

Sandia and AT&T have jointly developed a process for producing a 1.25-μm, double-poly, double-metal, radiation-hardened CMOS. Devices built with this process can be used in radiation environments that are several orders of magnitude more severe than those that can be withstood by similar, commercially available devices. By using an existing AT&T process as a baseline, this radiation-hardened process quickly showed acceptable product yields.

Functional, complex integrated circuits with excellent radiation tolerance were successfully built during the first two years of the program. Two examples of this successful joint venture are the SA3300 microprocessor, which incorporates over 70,000 transistors, and the 64-Kbit SRAM, with about 400,000 transistors.

Joint developments of this nature are greatly enhanced when the cooperating organizations use identical wafer fabrication equipment. If different equipment is used, the IC processes must be reengineered to achieve the same results. The use of identical equipment is supported by the semiconductor industry's trend toward combining prototype development and device production in the same facility.

Another key factor in this development was the face-to-face interaction between the semiconductor engineers at AT&T and Sandia, who combined their expertise to produce timely, technically correct solutions. The synergy generated by this collaboration enabled both organizations to achieve timely, cost-effective technical success.

References

1. R. R. Troutman, *Latchup in CMOS Technology—The Problem and Its Cure*, Kluwer Academic Publishers, Hingham, Massachusetts, 1986.
2. F. W. Sexton et al., "SEU Response of Design- and Resistor-Hardened D-Latches in the SA3300 Microprocessor," Sandia National Laboratories.

Biographies (continued)

development and for introducing AT&T's high-speed static and nonvolatile memory products to manufacturing. He received a B.S., M.S., and Ph.D. from Rensselaer Polytechnic Institute, Troy, New York, all in electrical engineering. Mr. Yaney joined AT&T in 1978.

(Manuscript received May 9, 1991)