# Quality Improvement Using Environmental Stress Testing

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AT&T and other leading manufacturers have developed techniques that use environmental stress testing to enhance the quality and reliability of electronics assemblies. These techniques consist primarily of applying thermal, vibration, and voltage stresses to components or assemblies during design and manufacturing. Environmental stress testing is a tool that is used to accelerate the detection of product weaknesses. When coupled with corrective-action programs, this tool also enhances product quality and reliability. This paper discusses applications of environmental stress testing in the electronics industry. It also reviews the results of environmental stress testing at AT&T's Little Rock Operations Center in Arkansas as applied primarily to the manufacture of circuit-card assemblies.

## Introduction

The quality and reliability of an electronics assembly is a function of the complexity of its design, the quality of its components, and the quality and consistency of the processes used to assemble it. During product design and development, one can improve an assembly's design margin and robustness by using accelerated stress techniques, coupled with failure-mode analysis (FMA) and corrective action. (*Design margin* refers to an extension of the specification limits for temperature, voltage, etc., to encompass a wider range than a customer will apply to the product. This makes the assembly more *robust*, i.e., able to tolerate wider variation in its operating conditions. Panel 1 defines acronyms and terms used in this paper.)

During assembly, the weaknesses caused by deficiencies in the components or in the assembly processes may degrade to become early-life failures, typically within the first six months of life. Usually, these weaknesses are mechanical defects, such as a broken integrated-circuit (IC) wire bond or a defective solder joint, that often do not show up when the assembly is first tested. However, because of the stresses that devices encounter during assembly and shipment and with the progression of time, the defects can show up as early-life or "infant-mortality" failures. By using thermal cycling and other stresses, one can identify these latent defects before shipment.

By itself, environmental stress screening (ESS) can be only partially effective. Few, if any, environmental screening techniques are 100-percent effective at finding all latent defects. In addition, if nothing is done to correct a problem at its source, the problem will often persist, and ESS will continue to miss some fraction of latent defects.

An ESS program is much more effective when combined with an aggressive FMA and corrective-action plan. AT&T prefers to use the term *environmental stress testing* (EST) when referring to such an approach, to emphasize the test and FMA and corrective-action aspects of the process. EST programs should be coupled closely with *total quality management* programs, which consist of process-improvement teams and partnerships with vendors, as well as other quality-improvement tools. (*Total quality management* is a management strategy that consists of heightened awareness of customer requirements, continuous process improvement, workforce empowerment, and management excellence.) As FMA uncovers the causes of the defects and the teams work to correct them, infant mortality will be brought under control. One can then move from EST on

**Panel 1. Abbreviations, Acronyms, and Terms**

100-percent EST — environmental stress testing on all assemblies

ASIC — application-specific integrated circuit

ASQC — American Society for Quality Control

CHMT — Components, Hybrids, and Manufacturing Technology Society

circuit card — a flat board that hold chips (dual in-line packages) and other components on the top side and has printed, electrically conductive paths in multiple layers for these components on its bottom side

constant failure — the assembly fails repeatedly with a constant threshold of failure above or below 25°C, yet within the established EST temperature range. (*Threshold* refers to the temperature where that unit repeatedly fails.)

CPU — central-processing unit

CRT — cathode-ray tube; often used to refer to a computer's entire video-display unit or monitor, not just the tube

cycles to failure — the thermal cycle where a failure first appears for a unit under test

DIP — dual-in-line package

discrete — an elementary electronic device (such as a capacitor, diode, resistor, or transistor) that is connected as a single part

DRAM — dynamic random-access memory

early-life failures — failures that typically occur within the first six months of the product's life

EPROM — erasable, programmable read-only memory

ESS — environmental stress screening; thermal, vibration, and voltage stresses are applied to a component or complete assembly during its design or early production

EST — environmental stress testing; testing while thermal, vibration, and voltage stresses are applied to a component or complete assembly during manufacture, coupled with failure-mode analysis and corrective action

FMA — failure-mode analysis; *failure mode* refers to the way a device failed during test or operation in the field. The *analysis* usually leads to identification of a failure mechanism that can be traced to a design, materials, or process defect

healer failure — sometimes called a self-healer; the assembly fails constantly or intermittently at all EST temperatures, and then begins to work normally at all temperatures for an extended period of time

IC — integrated circuit

IEEE — Institute of Electrical and Electronics Engineers

IES — The Institute of Environmental Sciences

intermittent failure — the assembly works sometimes but fails other times, somewhat randomly

motherboard — main system board of a microcomputer; usually contains the central-processing unit (CPU), random-access memory (RAM), support chips, and expansion slots for plugging in other circuit boards

pixel — picture element; the smallest display element (usually, a dot or cluster of dots) on a video-display screen

PC — personal computer

RAM — random-access memory

ROM — read-only memory

sample EST — environmental stress testing on some percentage of the assemblies

SMT — surface-mount technology

STRIFE testing — stress plus life testing, performed during design evaluation

UUT — unit under test

$V_{cc}$ — main dc circuit voltage

100-percent of the assemblies to EST on some percentage of the assemblies. (We refer to these as *100-percent EST* and *sample EST*, respectively.)

### EST During Product Design

It would be improper to discuss the manufacturing applications of EST without first examining its application to design.

An electronics assembly, such as a computer motherboard, is designed with operating specifications in mind; for example, an operating temperature range of 0°C to 55°C (degrees Celsius) and an operating voltage range of 4.75V to 5.25V (volts). Historically, designers have tested new products to the design limits and no further. The rationale was that no customer would operate the unit beyond those limits. Life testing was done on tens of units for months at a time, typically at an operating temperature of 55°C.

In 1982, the Hewlett-Packard Company began experiments with a concept that accelerated the process of life testing and referred to it as STRIFE (for *stress plus life*) testing.[1,2] The STRIFE test process exposes products to environments that are beyond the product's specification limits. It serves two purposes:

- *STRIFE testing adds design margin and robustness, as designs are changed to correct the faults it found.* Hewlett-Packard found that the same failure modes that occur outside the operating limits during design evaluation of small samples will occur later within the specification limits on a large population of the

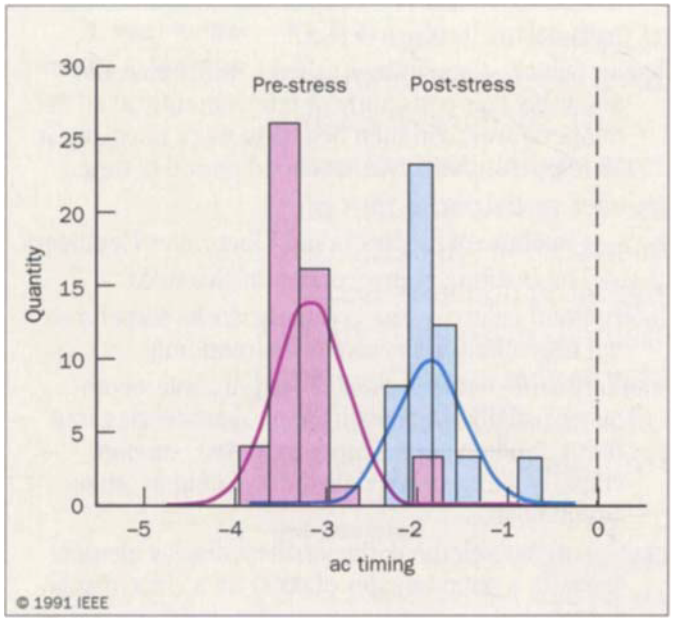


**Figure 1. Each device type has a typical distribution of key parameters. Here, we show the distribution of a device operating parameter for a sample of 100 integrated circuits, before and after environmental stress testing (EST).[3]**

product in the field.

- *STRIFE testing can be coupled with planning for EST in manufacturing.* The effectiveness of EST is enhanced when temperature excursions can be maximized, yet still allow a unit to operate without failure. This procedure provides greater stresses that increase the probability of detecting latent defects. However, false failures are undesirable and may occur if one exceeds the operating design limits.

Key parameters of electronic components can drift with time. Also, with large quantities of manufactured units, each device type has a typical distribution of key parameters, as illustrated in Figure 1.[3] These parameters may all be within a device supplier's specifications. But when this device is combined with other marginal devices in a circuit assembly, failures may occur within the assembly's operating limits. The probability is small that one will get only a few prototypes whose key parameters are near their specification limits. Therefore, marginal design issues may not show up if the units are tested only to the specification limits. This fact provides the motivation to "design in" margins for temperature and operating voltage.

In a STRIFE test program, one takes small samples (typically, fewer than ten units) during design verification and tests them to the specification limits. As a next step, the temperature, voltage, and vibration (and other factors considered important by designers) are increased in steps beyond the specification limits until failures occur. Every failure is analyzed, and action is taken to correct it.

At some point, the failure rate increases dramatically with small increases in stress. When this occurs, the fundamental design limits of the system have been exceeded and further stressing may not make sense. In one STRIFE test case, Hewlett-Packard has exposed a commercial product to temperature extremes of –55°C and 125°C, even though the product is specified to operate at 0°C to 55°C. Such extreme temperatures are environments usually reserved for rugged military products.

The Schmoo plot, a concept that was first developed in the semiconductor industry, can also be applied at the circuit-card level during STRIFE testing. Schmoo plots chart two key variables against each other to show the interaction between the variables.

This technique can be used to quantify and plot design margin for use in EST development. Figure 2 shows how a Schmoo plot can be applied to an electronics assembly, plotting test results (i.e., pass or fail) as a function of temperature and power-supply voltage.

In this example, the assembly passes all tests within specification, yet has insufficient margin below 5.0V and above 60°C to pass EST. Corrective action should be taken that would allow the design to function within the EST operating region (i.e., the larger shaded area in Figure 2). A quick check can be made by doing a "four-corner" test, i.e., by testing at the temperature and voltage settings at each corner of this region.

### Production EST

For production lots, the failure rate of specific infant-mortality defects is typically less than 5000 ppm (parts per million); i.e, 0.5 percent. This failure rate makes detection during STRIFE testing nearly impossible because of the small sample size. Therefore, 100-percent EST is required during early production. Later, with aggressive FMA and corrective action, one can reduce EST from a process that is applied to 100 percent of production to one that is applied to a sampling.

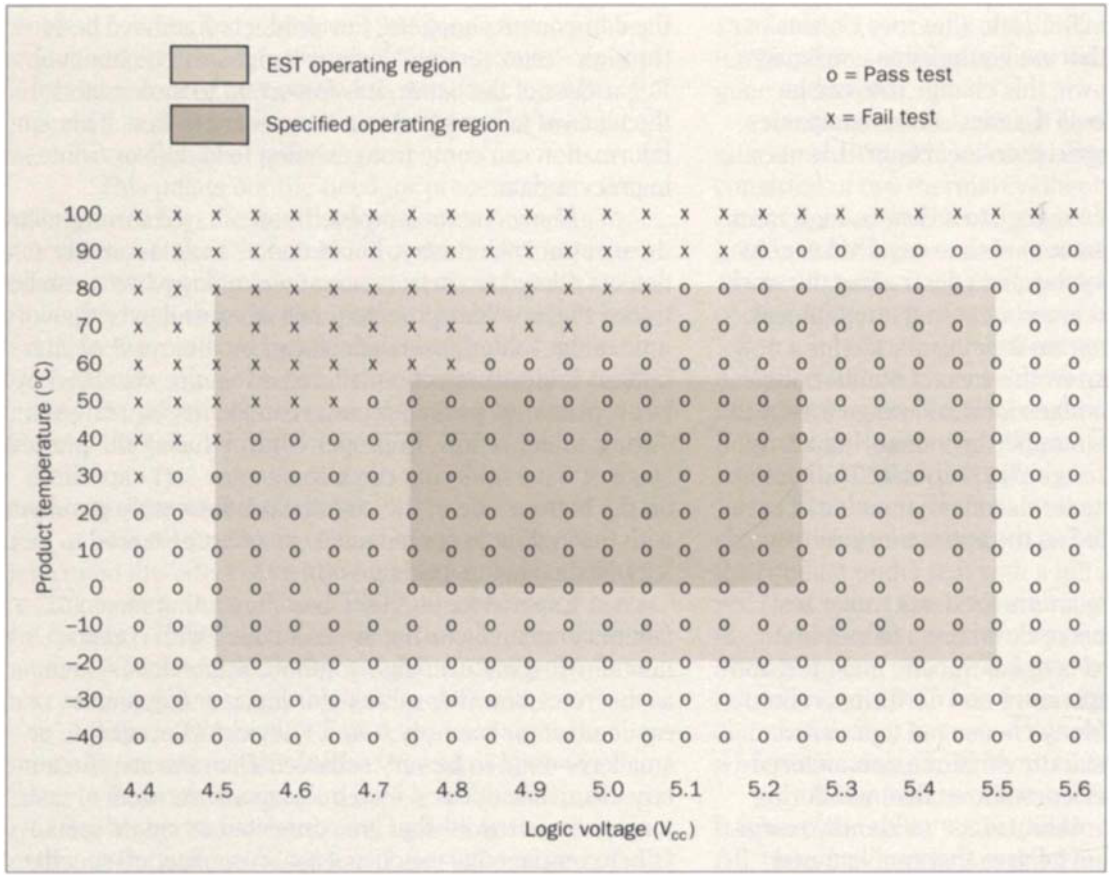


**Figure 2. This sample Schmoo plot for a computer motherboard can be used to establish maximum and minimum temperatures for a given voltage level in factory applications of EST. Clearly, design corrections are needed to enable this device to function within the EST operating region. A quick test using the temperature and voltage settings at the four corners of this region would verify the effectiveness of these corrections.**

Many in the electronics industry believe that EST can never be conducted effectively on a sampling basis.[4] However, sampling has been achieved and documented by AT&T and IBM.[5,6] Before sampling can be implemented, EST may be required for all units produced over a period of 2 to 6 months or for more than 10,000 production units to provide an experience base.

As the manufacturers of electronics assemblies implement total quality management in their own factories and ensure that their suppliers do the same, safeguards—such as sample EST—may no longer be required. Thus, with total quality management, they could go from 100-percent EST (for the early design and early production) to no EST.

**Techniques of Production EST.** The two primary techniques of production EST in use today are thermal cycling and vibration. Although both have their benefits, the most common technique applied in the commercial electronics industry is thermal cycling. Therefore, we have limited the discussion to that area.

Four key parameters are used when discussing thermal cycling:

- Temperature range ($\Delta T$)
- Temperature rate of change
- Number of cycles ($n$)
- Powered with test results monitored versus powered only versus unpowered.

The maximum allowable operating-temperature range for a product in EST is determined during the STRIFE process. This range should at least equal the operating-temperature specification range and, preferably, exceed the low and high ends of the specification range by 10°C or more.

The test-chamber facilities will limit the temperature rate of change. When a test-chamber system uses mechanical refrigeration with air as the heat-transfer medium, the product rate of change (i.e., the rate at which the product's temperature changes) typically will

be limited to 5°C/min to 20°C/min (degrees Celsius per minute). For chambers that are equipped to use liquid nitrogen to assist cool-down, this change rate can be increased to 25°C/min to 40°C/min.[7] Some companies are investigating even higher rates of change that use a liquid medium.[8]

In addition to increasing stress levels, high rates of change decrease the amount of time required to complete a given number of cycles, thus decreasing the work in process and the capital investment in EST equipment.

When an EST program is being started for a new product, it is difficult to know the correct number of cycles, *n*, to use. Typical values for *n* will range from 4 to 20. One can optimize this number by monitoring a large population of product through 20 EST cycles. The cycle for which the dropout rate levels off as a function of cycle number should be selected as the optimum cycle run time for that product.

The term *cycles to failure* for a unit under test (UUT) refers to the thermal cycle where a failure first appears. To know the cycles to failure, one must test and monitor results (i.e., temperature and device operation) during the EST process. Many choose not to monitor because of the cost of test fixtures. While unmonitored EST can be effective, experience shows that monitoring can more than double the ability of EST to identify marginal products.[9] Examples of failures that can be found only through monitoring are:

- *Intermittent* — the assembly works sometimes but fails other times, somewhat randomly.
- *Healer* — the assembly fails constantly or intermittently at all EST temperatures, and then begins working normally at all temperatures for an extended period of time.
- *Constant* — the assembly fails with a constant threshold of failure above or below 25°C, yet within the established EST temperature range. (The threshold refers to the temperature where that unit repeatedly fails.)

**FMA and Corrective Action.** Applying environmental stress techniques is only the first step toward improving quality and reliability. An even more crucial process to implement is that of FMA and corrective action.

During STRIFE testing, most of the corrective actions are changes made to the design; for example, parts selection, mounting techniques, and layout.

During production EST, corrective actions are typically changes made to the assembly process and with the component suppliers. For products that have been through STRIFE testing, design changes will be minimal. Regardless of the cause, it is important to understand the types of failures that EST is expected to find. This information can come from existing field data or from in-process data.

Many common problems are shared throughout the electronics industry. For instance, most assembly defects related to surface-mount technology (SMT) can be traced to the solder process. Lack of control over the volume of the solder-paste deposit can be the cause of intermittent solder-connection failures. Moisture absorbed by large, plastic, IC packages can create damaging stresses during solder reflow. Improper control during the preheat stage of wave soldering can also damage SMT capacitors on the bottom side of the circuit card. Assembly problems with through-hole components can often be traced to bent legs on dual-in-line packages (DIPs).

Experience at AT&T has shown that most EST failures in manufacturing are associated with components.[9] Most mature, high-volume components—such as discretes, transistor-transistor logic, and dynamic random-access-memory (DRAM) devices (1 megabyte or smaller)—tend to be very reliable. (*Discretes* are elementary electronic devices—such as capacitors, diodes, resistors, or transistors—that are connected as single units.) Other components—such as custom application-specific integrated circuits (ASICs), hybrids (especially oscillators), and printed-wiring boards—need the most attention. Also, what may seem to be an SMT solder defect may, in reality, be caused by poor solderability of a component lead or a board solder pad. (*Solderability* refers to the ability of the lead or pad to be soldered.) Lead planarity is also critical for SMT plastic-quad-flat packs and plastic, leaded-chip-carrier packages. Nonplanar leads may result in intermittent contact between the lead and the solder fillet.

Once an EST program has been set up and begins to identify defects, it is crucial that FMA of these defects be performed as soon as possible. If a supplier problem is identified as the cause, then it is primarily the supplier's responsibility to identify the design feature or process step that is responsible for the defect and take action to prevent recurrence. This action is necessary for an EST program to be most effective.

Accurate data collection plays a critical role in a program of improvement. While the cause of a 1000-ppm

problem is being tracked down, 999 good pieces will be produced for every defective one. Not only must every defect be recorded accurately in a database, it is also important to remove the part carefully, save it, and document its conditions of failure.

This points out the need for process teams (i.e., solder, assembly, etc.) and component engineering to stay abreast of the EST results. Process-quality improvement teams typically drive corrective action on all process-related defects. Component teams typically collect defective parts and work closely with the suppliers to identify the failure mechanisms, and define and commit to the plans of action required to prevent recurrence of the failures.

### Production EST Studies at AT&T

Several studies have been done at AT&T to determine the effect of EST on outgoing-product quality, i.e., to measure the quality of the product before it leaves the factory.[5,9] This section summarizes the approaches taken at AT&T's Little Rock Operations Center, while the next section summarizes the results achieved.

Efforts within AT&T were directed to further improving customer satisfaction. In addition, we were trying to improve the existing card-level burn-in process by using higher stress levels and by adding functional testing to the process. Card-level burn-in consisted of power-only (i.e., unmonitored) temperature exposure at 50°C to 70°C for 12 to 72 hours.

The products studied were terminal-controller circuit-card assemblies and computer motherboards that were assembled using combinations of surface-mount and through-hole technology. All the products were controlled by a microprocessor and included on-board test diagnostics in firmware, i.e., software that is programmed into read-only memory (ROM).

The EST evaluation program included extensive FMA of the defects identified, and close interaction between component suppliers, line engineers, and the operators who were responsible for circuit-card assembly. In several instances, the design group became involved in the analysis and corrective-action process. No products studied from 1988 through 1991 had been through a full STRIFE testing program during design.

The ability to test assemblies while stress environments were being applied enhanced the program's success. Not only could we determine the optimum EST duration, we could also find many intermittent and temperature-sensitive failures that might otherwise have gone undetected.

**Facilities Hardware and Software.** During the first quarter of 1988, evaluation facilities were installed that consisted of two thermal-cycling chambers with roll-in carts for associated test fixtures. The chambers could hold up to 12 fixture shelves, each able to hold up to 16 circuit cards. Each chamber had a single-stage, water-cooled, 30-horsepower compressor.

In 1989, the chambers and fixturing were redesigned and additional chambers were installed. The chamber capacity was increased to 16 shelves that could hold up to 24 cards each. Typical EST production runs consisted of 200 circuit cards.

In the original chambers, the average rate of change during temperature pull-down, as measured on the product under test with a full production load, was 9°C/min over a temperature range of 80°C to 0°C. When the minimum temperature was extended to –20°C, the average rate of change dropped to 6°C/min. The pull-up rate averaged 10°C/min from –20°C to 80°C. The new chamber design increased the pull-up rate to 18°C/min, while maintaining roughly the same pull-down rate.

A key feature of the system designed by AT&T has been the ability to test and log results (i.e., pass or fail, time, and temperature) automatically while stressing the assemblies. One series of terminal-controller products relied on the communication of self-test results over a multiplexed data line. All video-controller products, including PC motherboards, are tested using a test board that is referred to as a *pixel counter.* (*Pixel* stands for picture element. It is the smallest display element—usually, a dot or cluster of dots—on a video display screen, such as a CRT.) The pixel counter replaces the CRT by counting the video-pixel transitions during one vertical sweep made by the CRT control circuitry in the UUT. Pixel counts for up to 16 cards at a time are then transmitted to a computer, where custom software compares the counts for each UUT to that of video-controller cards that are known to be good.

During a typical production EST run, a UUT is tested and results are reported up to 150 times over an 8- to 12-hour period. A separate computer file is maintained for each UUT, and results are recorded as a function of time and temperature. Results for a given UUT are plotted to show time, temperature, and pass or fail status,

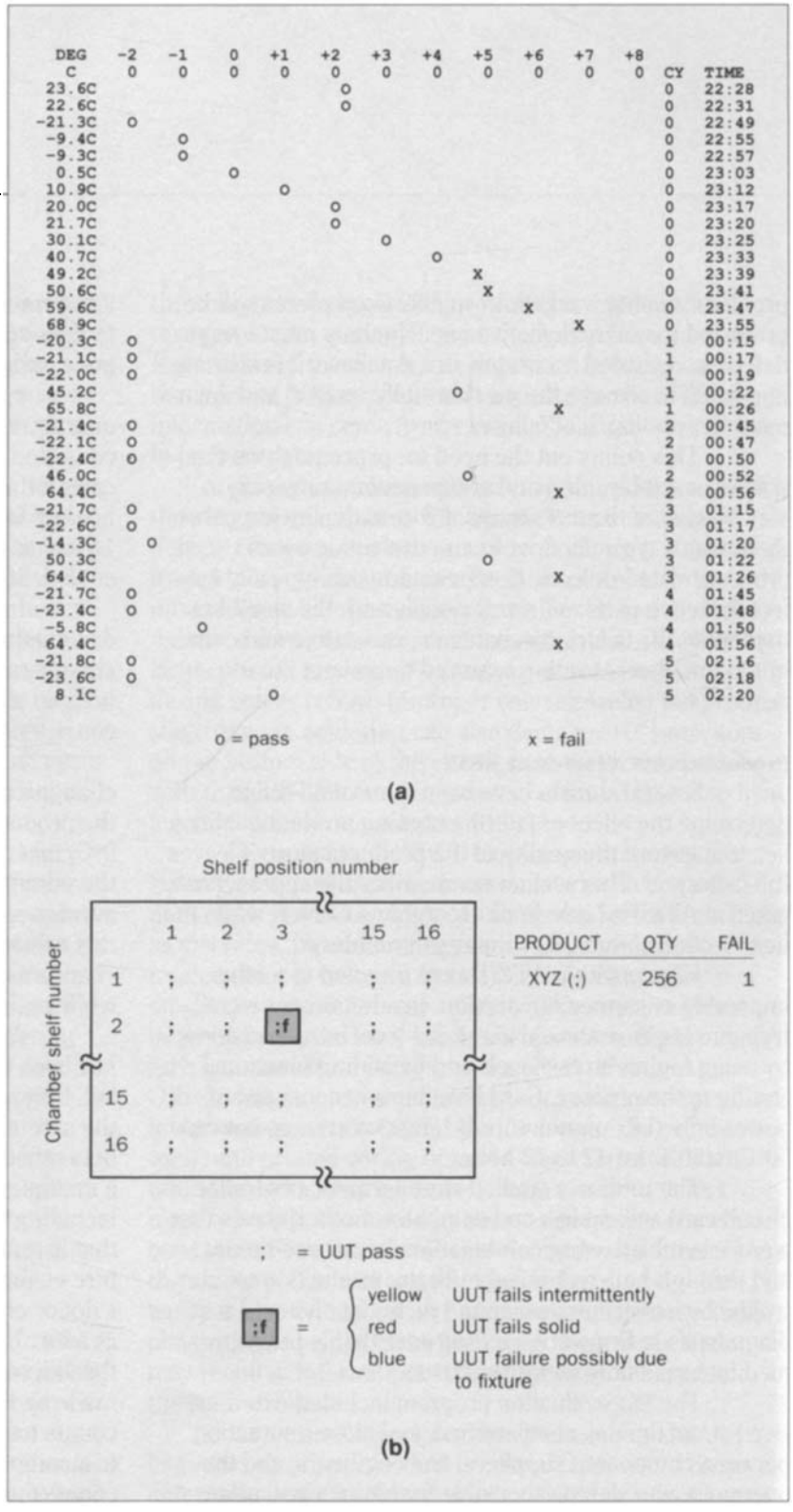


**Figure 3. Test results for each unit under test (UUT) in the thermal-cycling chambers were maintained in a separate electronic file. (a) Typical plot of failure versus time and temperature for a single UUT, where O = pass and X = fail. The CY column identifies the cycle number. This unit has a threshold of failure equal to 50°C. (b) A color terminal serves as a monitor and provides real-time status information about the current run. Each element in the array on the terminal's display represents a UUT. The character in each array position identifies the card type, and appears in green if the unit passed the test. Other colors indicate a failure. Data about the product under test appears to the right of the array.**

along with specific pixel counts. (Figure 3a shows a typical plot. The temperature range for the test serves as column heads, and the CY column gives the cycle number. The O and X denote pass and fail, respectively, and are determined by software from the pixel counts.)

A color terminal located next to each chamber door serves as a monitor and provides real-time status information about the current EST run (Figure 3b). The monitoring terminal displays an array of 16 horizontal rows with 16 columns. Each element in the array represents one UUT. A computer file for each unit contains a pixel count for each test of the unit in this EST run. Thus,

each horizontal row represents a pixel counter, while each of the 16 positions in the row represents a slot on the pixel counter.

The type of card being tested in a shelf–slot position in the chamber appears as a character in the corresponding row–column position of the monitoring terminal's display. The color of this character identifies the condition of the card being tested:

- *Green* for pass
- *Yellow* for intermittent failure
- *Red* for hard failure (as opposed to an intermittent failure); sometimes called a solid failure.

In addition, *blue* indicates a UUT failure, but identifies the slot as possibly a bad test position. It means that three units have failed in that slot in the last seven EST runs. If these units pass when retested in other slots, then the test position is suspect.

**Thermal Profile.** All thermal-cycling EST runs on circuit cards followed the same basic guidelines. A profile consists of two parts: step stress and *n* rapid thermal cycles, where *n* depends on the product being tested.

For step stress, all profiles begin with an initial test at 25°C in the chamber; power is then turned off, and the temperature is pulled down to –20°C. This represents the first iteration of step stress. After at least one test, the temperature is increased 10°C, with power turned off. Units are once again powered on and tested.

This process is repeated up to the maximum setpoint temperature, typically 70°C to 80°C. (Each product family has a different setpoint.) The step-stress sequence takes a maximum of 2 hours.

When step stress has been completed, the *n* rapid thermal cycles begin. Each cycle goes from –20°C to the maximum setpoint and takes a half hour to complete. Power is off during the temperature pull-down, and on during the pull-up. Figure 4 shows typical thermal profiles used.

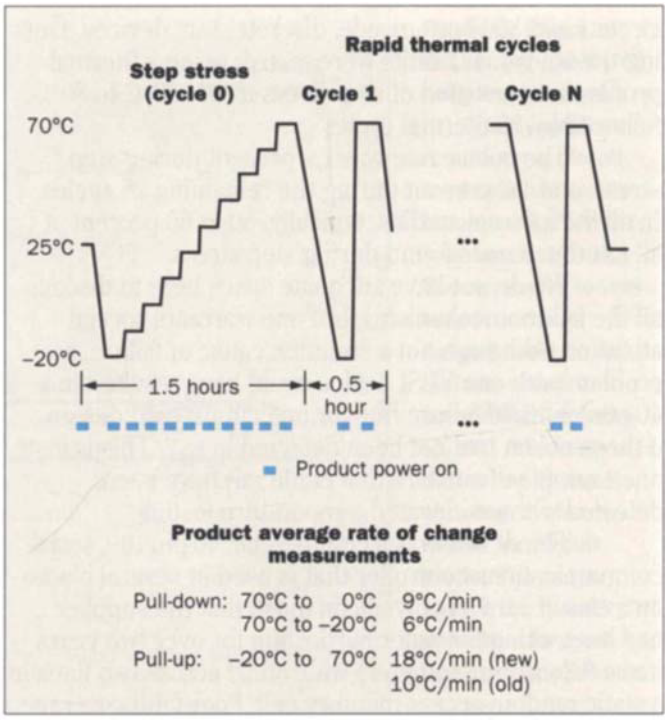


**Figure 4. The thermal stress studies conducted at AT&T followed a thermal-cycle profile similar to this one for temperature (top) and power during step stress and rapid thermal cycling. The heavy bars below the temperature curves show when power was on during the cycle.**

## Results of Thermal-Cycling Studies

Here, we summarize the results of thermal-cycling studies on five circuit-card product families. All Phase I through III work was done in the two original EST chambers, while the Phase IV work was done in the new chambers with a higher temperature pull-up rate.

**Phase I Study.** Phase I was designed to evaluate the effectiveness of thermal cycling with no power applied to the product. As a separate part of the experiment, the product was also manually tested at a functional test bench at temperature extremes of 0°C and 80°C, before and after thermal cycling.

Although ten unpowered thermal cycles from –20°C to 80°C alone did precipitate hard failures, many defects were found only because of the testing done at temperature extremes. In addition, there was no way to verify the optimum number of thermal cycles.

These issues became the main driving factors to automate the acquisition of test data from the EST process, starting the second quarter of 1988.

**Phase IIa.** By using a product's built-in self-test in the chambers, we could address both the high cost of doing temperature tests on one unit at a time and the need for time-to-failure data during EST.

The product studied in Phase IIa consisted of three board designs. The boards measured 11 inches by 14 inches and contained more than 100 DIP integrated

circuits and 300 bottom-side, discrete, SMT devices. During the study, 5172 units were tested, using a thermal profile that consisted of step stress from –20°C to 80°C, followed by 25 thermal cycles.

The failure rate was 1.9 percent during step stress, and 1.2 percent during the remaining 25 cycles. In all the internal studies, typically, 50 to 65 percent of all EST defects are found during step stress.

We do not have adequate space here to discuss all the failure mechanisms, but one warrants special attention. Although not a common cause of failure, a problem with one VLSI device could have resulted in a 40-percent field-failure rate for one circuit-card design, if the problem had not been detected in EST. This is just one example of a failure that could not have been detected without elevated temperature testing.

The device was a commercial, 40-pin DIP, serial-communications controller that is used in several places on a circuit card. A polysilicon mask that the supplier had been using for wafer fabrication for over two years had a 0.2-μm (micrometer) wide short across two lines in a static random-access-memory cell. Poor fault coverage prevented the supplier from detecting the defect during test. Because of the location of the short, failures occurred only when the product was operated above 40°C. This worst-case example of a catastrophic defect would never become a "hard" failure at 25°C, yet it presented a major risk for customers.

Phase IIa was also used to measure EST's effect on the outgoing quality of the product being manufactured at Little Rock. The results of outgoing-quality audits before and after EST implementation showed a two to four-fold reduction in functional failures. The data presented in Figure 5a reflects functional failures only and does not include visibly detracting features or mechanical defects that do not contribute to functional failure. In addition, this phase provided a measure of the cycles to failure, which was then used to optimize the EST duration at 16 cycles for subsequent production. (See Figure 5b.)

**Phase IIb.** Although the quality-audit data acquired in Phase IIa was helpful, field data was needed to provide information to show if EST also affected our customers' view of the quality of our products. Another product was studied using the pixel-counter design. The product consisted of three circuit cards that used through-hole technology and were designed around a 16-bit microprocessor.

Initial production runs without EST were tracked to determine out-of-the-box and first-month failure rates. (*Out-of-the-box failure* means the product failed on its first use. *First-month failures* are those that occur during the first month of operation.) Then, production runs with EST were tracked, and the failure rates were compared.

A population of units that had not been through burn-in or EST was tracked to one customer. Thereafter, all products to be shipped to this customer went through 20 thermal cycles from –20°C to 80°C while test results were monitored. An EST failure rate of 9.9 percent was measured for these units.

The first-month quality measured showed a fivefold improvement between the non-EST and EST units. While this study pointed out significant field-quality improvement, it also revealed that some failures escape detection in EST. For example, two 512-kilobyte EPROMs (erasable, programmable read-only memories) failed in the field. Here, EST testing had been done at $V_{cc}$ levels of 5.0V plus or minus 5 percent. This EPROM failure involved degradation of a gate oxide, which could have been detected at higher $V_{cc}$ levels (i.e., 5.2V to 6.5V).

Other examples of potential failures that may escape detection in EST are software-application failures and failures attributed to shipping damage or electrical overstress.

Another failure mechanism, referred to as a healer, was found in EST and warrants discussion. The interface between a 1-megabyte, DRAM, single in-line memory module and the socket failed at a rate of 10,000 ppm (i.e., 1 percent). All EST failures occurred within the first two cycles. By the seventh cycle, the failures had totally healed, only to reappear intermittently within a few days after EST.

As is true with most healers, an oxidized mechanical interface that originally showed electrical continuity at 25°C will open in one thermal cycle because of differences in the coefficients of thermal expansion between the module and socket. With multiple cycles, the oxides at the interface crumble and allow metal-to-metal contact. After EST, with further exposure to air, the interface reoxidizes and, once again, opens electrically. This is a common symptom of intermittent solder joints.

**Phase III.** The purpose of Phase III was to evaluate the feasibility of EST sampling. A mature circuit-card design that was manufactured using through-hole technology was selected to evaluate sampling effectiveness.

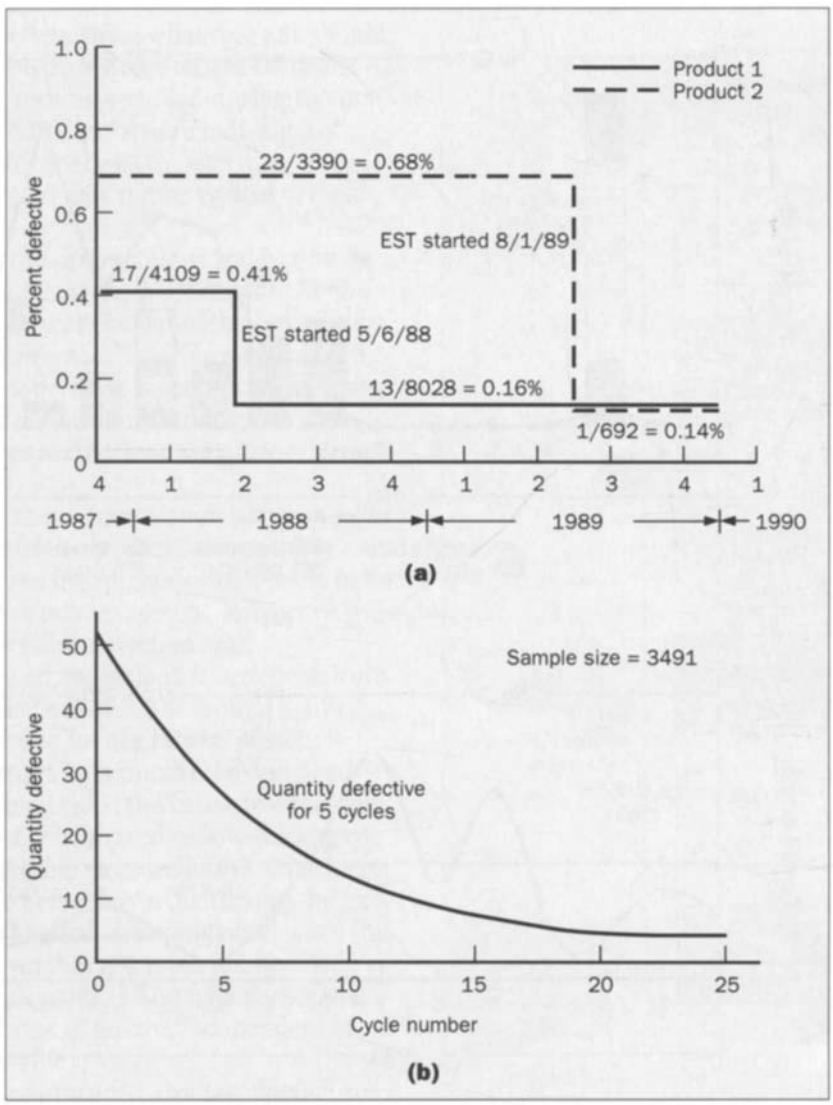


**Figure 5. Effect of EST on the quality of outgoing product. (a) Quality-audit results on a circuit-card product family before and after EST was implemented. These results reflect only functional defects, and do not include visual or mechanical defects. (b) EST failure distribution for Phase IIa, showing cycles to failure for circuit cards. The curve shows the quantity defective for each five-cycle increment.**

The circuit card had 30 integrated circuits and 129 discrete components, designed around an 8-bit CPU. The EST profile consisted of 20 cycles from –20°C to 70°C, preceded and followed by a 25°C functional test. While testing was done on all UUTs in EST, fault coverage was limited to less than 30 percent (i.e., fewer than 30 percent of the potential faults could be identified with the electrical test in EST).

The purpose of sampling is to reduce manufacturing costs without adversely affecting warranty costs or customer satisfaction. A break-even point for costs occurs when the EST-dropout rate falls and remains below 0.5 to 1.0 percent, depending on the cost of the warranty and the cost of performing EST.[10] The EST-dropout rate can consistently be reduced below these levels only if aggressive FMA and corrective-action programs are carried out successfully.

During March 1989, a sample of the product was run in EST, where a 2.5-percent dropout was measured. In September 1989, all of this product began going through EST. The plan called for 100-percent EST until the dropout on 1000 consecutive units was below 0.5 percent. This lower dropout rate occurred in January 1990. EST sampling began at 50 percent in February, and was

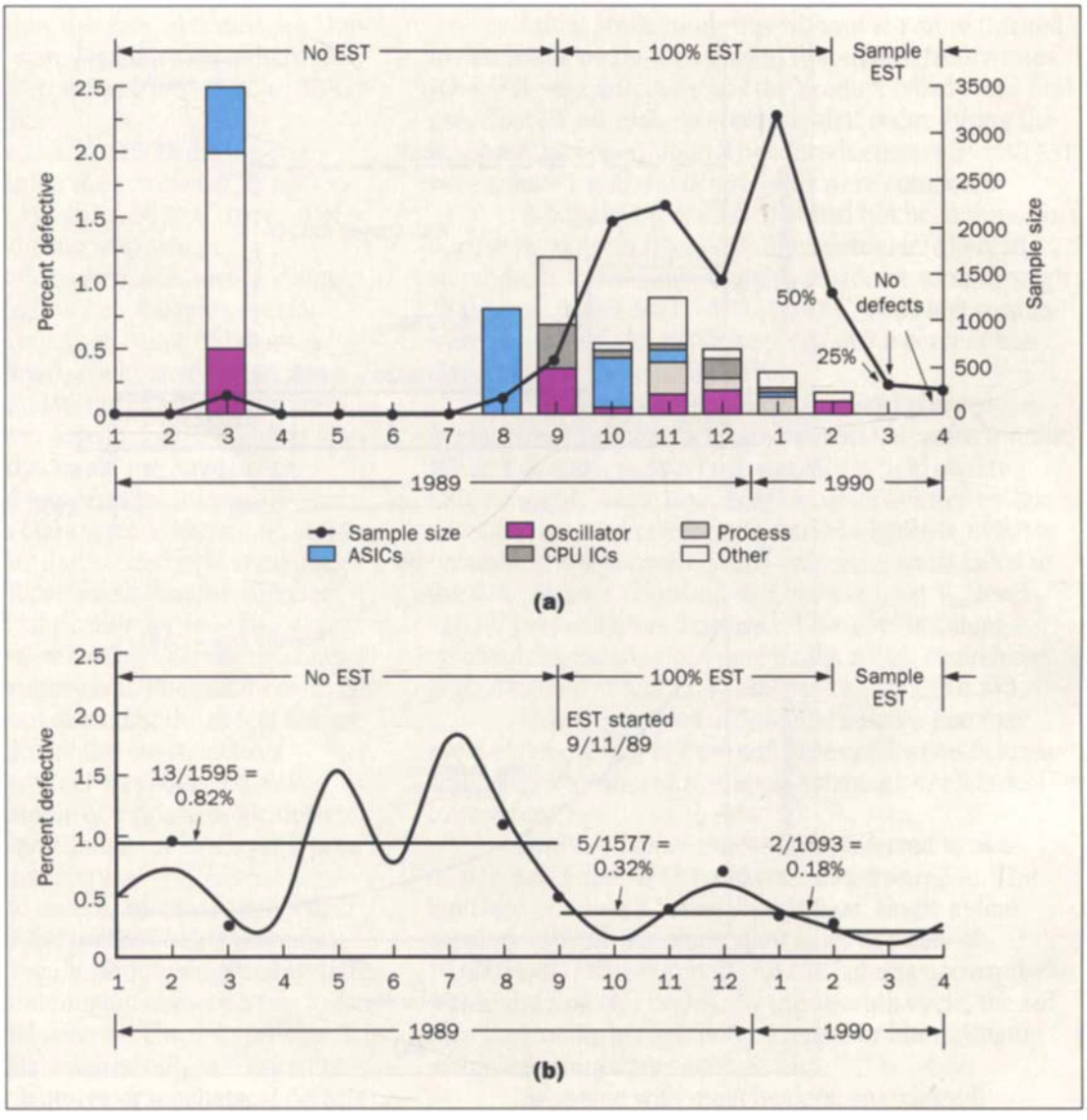


**Figure 6. Phase III EST-sampling feasibility study. (a) Percent defective in EST, separated according to defect category. (b) Quality-audit results on outgoing circuit cards before EST was implemented, during 100-percent EST, and during sample EST.**

reduced to 25 percent in March and April. The study ended in May 1990 because the factory stopped manufacturing the product.

Figure 6a tracks results during the project, while Figure 6b shows the corresponding outgoing-quality-audit results for the same period. Before 100-percent EST was implemented, the quality was erratic, averaging 0.82-percent defective. Even with 100-percent EST, the outgoing-quality-audit results still averaged 0.32-percent defective, which was unacceptably high for a mature technology of this complexity. Part of the reason for this high failure rate was the limited ability to test the assemblies in EST. The quality-audit results did not achieve an acceptable level until all the major failure mechanisms had been eliminated.

This crucial evidence after two years of investigations proved that the most effective part of an EST program is not the process of stress testing, but rather the effectiveness of the actions taken to rectify the problems found.

**Phase IV.** The most recent investigation dealt with EST on PC motherboards that an outside supplier assembled. The supplier shipped its product with a guaranteed out-of-the-box quality level of under 0.5-percent defective. More than 17,000 motherboards were tracked

over a 4-month period to determine what role EST should play, if any. The study also provided a way to compare EST failure mechanisms with those found during the out-of-the-box test to see if EST failures were indicative of true early-life defects. The goal was to determine if the EST precipitated defects that may not be typical of those that customers see.

Figure 7 shows the product flow, and Figure 8a shows the out-of-the-box quality and EST results. At no point in the 4-month study was the out-of-the-box quality within the 0.5-percent guaranteed limit. In addition, EST identified as defective another 4 to 9 percent of the units that would otherwise have been shipped to customers. As with the earlier studies, extensive FMA was performed on all defects.

FMA results did show a correlation between failure mechanisms seen at out-of-the-box test versus those found in EST. Figure 8b compares the quantities of defects in five categories of failure at the two test points. Reference 9 discusses details of specific failure mechanisms.

Figure 8a shows an anomalous failure peak from weeks 8 through 11. This peak resulted from a 4- to 6-percent failure rate for one lot of a 68-pin, plastic, leaded-chip-carrier package. FMA uncovered damaged IC-package wire bonds and traced the cause to excessive package moisture during the infrared-reflow-solder process, which created excessive stresses in the IC package.

While EST proved effective in identifying the existence of this failure mechanism, data published since this study was done has shown that EST must not be used simply to screen out weak parts.[11] The data shows that there is an even greater risk of failure, independent of EST, later in the product's life.

**Future Studies.** In future EST studies, the failure rates and mechanisms found for environments with a temperature rate of change of 10°C/min to 20°C/min will be compared to those found for environments with liquids at 50°C/sec (degrees Celsius per second).

Efforts will continue toward improving the efficiency of the FMA process, including closer partnerships with suppliers and agreements on faster resolution of problems.

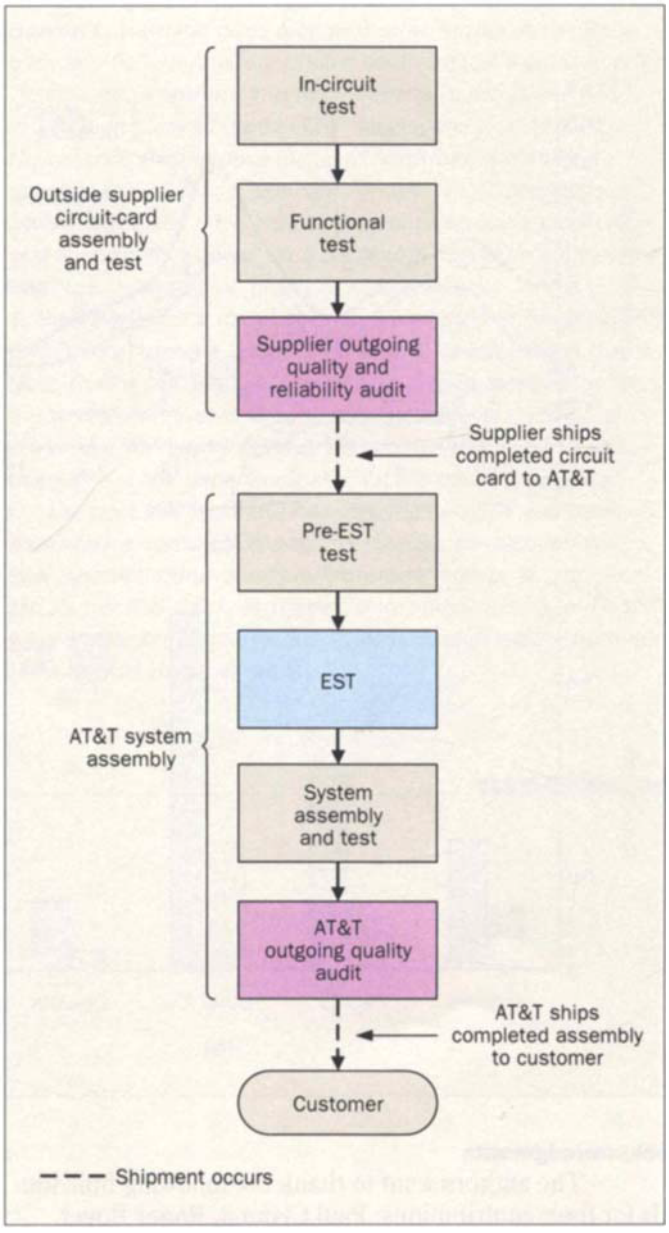


**Figure 7. Product flow for a PC motherboard. The supplier had guaranteed an out-of-the-box quality level of fewer than 0.5-percent defective units.**

## Conclusion

A successful manufacturing EST program begins during product design using STRIFE testing techniques. Once introduced into manufacturing, EST should immediately become a tool for providing insight into component and process weaknesses. It should not be relied on as a screen, but as a process-control tool. Proper use of the tool should decrease the reliance on EST and increase the reliance on control of assembly and supplier processes as a way to improve product quality and reliability.

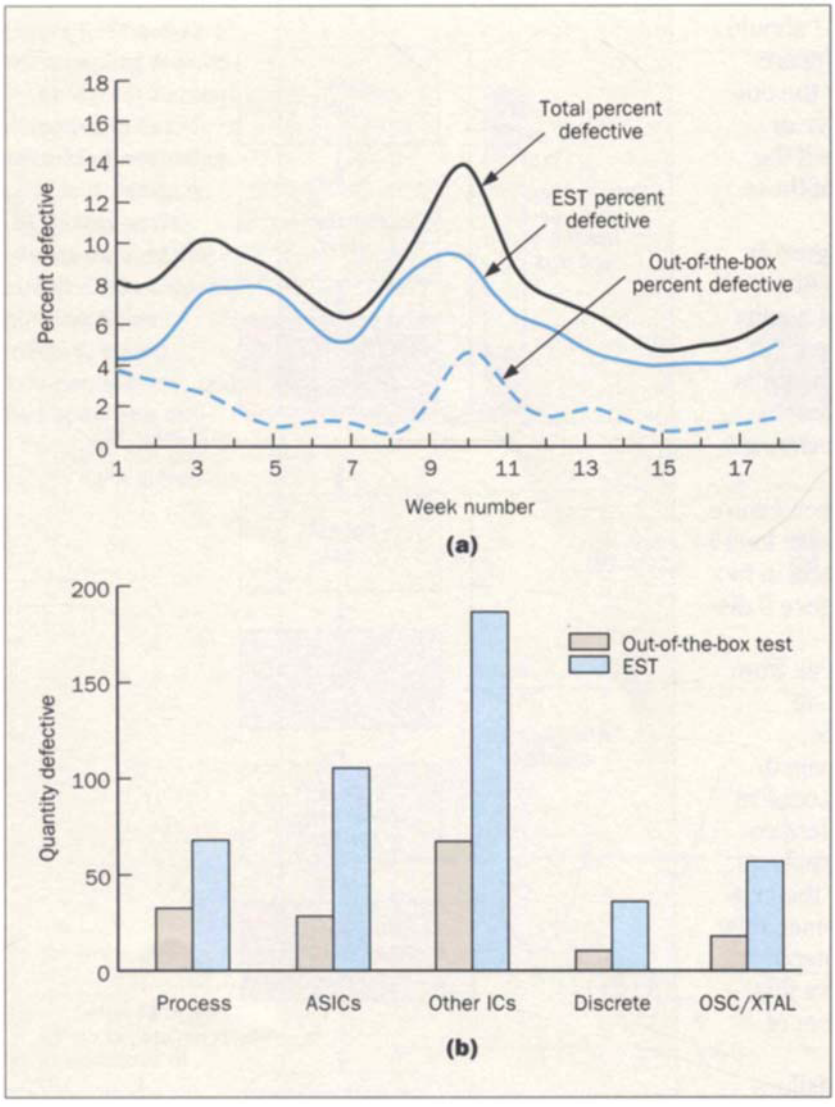


**Figure 8. The PC motherboards were evaluated over a four-month period at AT&T. (a) Failure rate at AT&T. At no point did out-of-the-box units meet the supplier's guaranteed quality level. Also, another 4 to 9 percent that might have been shipped in systems were identified as defective during EST. (b) Quantities defective before and after EST was implemented. Failure-mode-analysis results showed a correlation between failure mechanisms during out-of-the-box test and those found in EST.**


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## References


1. C. Suesy, "Achieving Phenomenal Reliability Growth," *ASM 1987 Conference on Reliability—Key to Industrial Success*, Los Angeles, California, March 24–26, 1987, ASM International, Metals Park, Ohio, 1987, pp. 79–88.
2. C. Shinner, "The Board Electronic STRIFE Test (B.E.S.T.) Program," *ASQC Reliability Review*, Vol. 8, No. 2, June 1988, pp. 3–6.
3. B. Cole et al., "Statistical Product Monitoring: A Powerful Tool for Quality Improvement," *1991 International Test Conference Proceedings*, Nashville, Tennessee, October 26–30, 1991, IEEE Computer Society, Test Technology Technical Committee, IEEE International Test Conference, Altoona, Pennsylvania, 1991, pp. 446–453.
4. S. F. Scheiber, "The New Approach to Environmental Test," *Test & Measurement World*, Vol. 9, No. 9, September 1989, pp. 71–76.
5. T. P. Parker and C. W. Webb, "A Study of Failures Identified During Board Level Environmental Stress Testing," *Proceedings, 42nd IEEE/CHMT Electronic Components and Technology Conference*, San Diego, California, May 18–20, 1992, Components, Hybrids, and Manufacturing Society, IEEE, New York, New York, 1992, pp. 177–184.
6. W. R. Wright, "Successful Stress Testing at IBM, Greenock, Scotland," presented at the 1991 IES Annual Technical Meeting, San Diego, California, May 6–10, 1991, The Institute of Environmental

Sciences, Mount Prospect, Illinois. For a copy of this paper, contact the author at IBM (UK) Ltd., Spango Valley, Greenock PA 16 OAH, Scotland.
7. S. A. Smithson, "Effectiveness and Economics—Yardsticks for ESS Decisions," *1990 IES Annual Technical Meeting*, New Orleans, Louisiana, April 23–27, 1990, The Institute of Environmental Sciences, Mount Prospect, Illinois, 1990, pp. 737–742.
8. B. Beaton, "Thermal Accelerated Reliability Go–No-go Environmental Testing (TARGET) Dynamic Board Thermal Shock Using a Single Fluid and Bath," *Eleventh IEEE/CHMT International Electronics Manufacturing Technology Symposium: The Keys to Manufacturing in the 1990's*, San Francisco, California, September 16–18, 1991, Components, Hybrids, and Manufacturing Technology Society, IEEE, New York, New York, 1991, pp. 212–214.
9. T. P. Parker, "ESS Case Study of a High Density Surface Mount Circuit Card," *1991 IES Annual Technical Meeting*, San Diego, California, May 6–10, 1991, The Institute of Environmental Sciences, Mount Prospect, Illinois, 1991, pp. 393–402.
10. C. Haibel, "Math and Economics of Screening Disk Drives," *1990 IES Annual Technical Meeting*, New Orleans, Louisiana, April 23–27, 1990, The Institute of Environmental Sciences, Mount Prospect, Illinois, 1990, pp. 784–788.
11. T. M. Moore et al., "The Application of Scanning Acoustic Microscopy to Control Moisture/Thermal Induced Package Defects," *ISTFA 1990: International Symposium for Testing and Failure Analysis*, Los Angeles, California, October 29 to November 2, 1990, ASM International, Metals Park, Ohio, 1990, pp. 251–258.

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