Three-Dimensional Imaging for Circuit-Board Assembly

Israel Amir
Frank P. Higgins
John B. Macdonald
Howard N. Gaston
Rodney E. Griffin

A major barrier to improved process control in electronic circuit-pack assembly is the lack of robust, high-speed, cost-effective sensing technologies. As part of an overall process-control system, AT&T's Little Rock (Arkansas) Operations Center is implementing a new three-dimensional (3-D) imaging system that measures the amount of solder paste applied to circuit boards. The system uses an imaging technique that can measure the solder-paste volume of each site on a circuit board at production rates. Our investigation shows that solder-paste volume is an important process-control parameter for high-quality circuit board assembly.

Introduction

Advances in miniaturization technology have introduced significant challenges to electronic assembly. Since the introduction of surface-mount (SM) technology, industry has increased the number of solder interconnections on circuit boards. (See Panel 1 for definitions of abbreviations, acronyms, and terms.) At the same time, the size of leads and the spacing between interconnections are shrinking, raising the incidence of short circuits and leads with insufficient solder.

A poor solder joint may be the result of poor land-lead surface finish, insufficient solder, inappropriate reflow soldering temperature, etc. Electrical testing, the main source of today's process and defect information, is performed after the circuit board is assembled. However, electrical testing requires expensive equipment and support operations, and it can only verify that the board satisfies a set of electrical criteria at a particular time. Marginal solder joints, which subsequently can fail because of mechanical stress and corrosion, are usually electrically indistinguishable from good solder joints. When a marginal solder joint is found during testing, there is little time for *root-cause-analysis*. Because test results cannot be correlated directly with the individual processes that precede them, testing provides little useful data regarding the *quality* of assembly. Further, it is conducted too late to be applicable to closed-loop process control.

Zero-defect manufacturing requires monitoring the quality of an on-line process and establishing appropriate closed-loop control to detect changes and correct process drifts before a marginal product is produced. Improving the quality of a product before it is tested can also reduce testing costs.

To achieve and maintain high-quality SM circuit-pack assembly, we must maintain tight process control of the three basic operations: solder-paste deposition, device placement, and reflow soldering. Although significant advances have been made in placement technology, advances in paste deposition and reflow have been less dramatic. Solder-paste deposition, a screen-printing process that covers each SM land with paste, is a critical step in SM assembly. Solder-paste volume and registration are considered the key printing parameters. To attain zero defects, every paste deposit on the board should be monitored. However, it is impractical to measure the volume of paste on each land accurately with existing technologies at production rates. The fastest available systems use 3-D laser triangulation. They are about ten times slower than is required to attain 100-percent inspection of solder-paste volume on AT&T products.

Recently, scientists at AT&T Bell Laboratories conceived a new approach to 3-D imaging. It is much faster than existing methods and has the potential to provide 100-percent in-line solder-paste volume measurement. A beta-site system based on the AT&T

Panel 1. Abbreviations, Acronyms, and Terms

beta site—user test site

CAD/CAM—computer-aided design/computer-aided manufacture

ERC—Engineering Research Center

land—A metallized area on a circuit board on which a device lead is placed.

SM—surface mount

solder paste—A slurry of microscopic solder balls mixed with a viscous binding flux.

solder-paste reflow—A process for joining parts by tinning the mating surfaces, placing them together in solder paste, heating until the solder fuses, and cooling in the joint position.

through-hole technology—An interconnection technology in which device leads are soldered into electrically conducting holes in a circuit board.

Bell Laboratories development prototype was built by engineers at the Little Rock Operations Center to investigate how solder-paste volume and registration correlate to solder-joint defects. In this paper, we outline the new 3-D imaging concept and its system architecture. We also review some initial results of factory investigation and discuss future work.

3-D Intensity Ratio Sensing

Our machine vision group at AT&T Bell Laboratories has been developing process control and inspection methods for circuit-board assembly since 1982. During this time, we designed a circuit-pack inspection system based on a line-scan camera, which consists of a single row of image-sensing elements (pixels) and associated electronics, integrated with an appropriate lens system.[1] In this system, a camera gathers contiguous line images during controlled relative motion of the scene to create two-dimensional (2-D) image data. The system has been applied in AT&T factories to verify lead presence in through-hole technology and to assess solder-paste and component registration in SM technology.

As SM technology evolved, the need for high-speed, 3-D sensing became critical. We have developed and will describe a method based on a line-scan camera and intensity ratio sensing that has the potential to meet this need. J. Schwartz[2] first proposed the fundamental principle of 3-D imaging using intensity ratio sensing based on 2-D area camera technology.[2–4] In this approach, an illumination gradient (in which illumination intensity varies spatially) must cover the entire 2-D image area. This severely limits measurement performance, especially for electronic assembly applications. In addition, the line-scan technique offers a substantially simpler calibration procedure.

To describe our method, consider a single pixel in a line-scan camera (see Figure 1a). We first create a positive illumination gradient in the z direction. The intensity at position Z' for this condition is I'_1. Next, we change to a negative illumination gradient. The intensity at Z' for this condition is I'_2. If we move the point of interest to a new z position, Z'', the new intensities are I''_1 and I''_2, as shown in Figure 1a.

If we assume, for the moment, that the illumination profiles are linear and the reflectance remains constant for the two lighting conditions, the intensities received by the camera for the given pixel at any height z can be expressed as:

$$I_1 = K\,(a_1 z + b_1) \tag{1}$$

$$I_2 = K\,(-a_2 z + b_2)$$

where I_1 and I_2 are the intensities for the two illumination conditions, respectively; K is the reflectance of the point to be measured; z is the height; and a_1, a_2, b_1, and b_2 are the respective slopes and intercepts of the linear-light-intensity profiles. The reflectance, K, for a given point on the object is a function of incident illumination and viewing angles. K remains constant if these angles are unchanged for the two illumination conditions. Dividing the two equations above results in:

$$R = \frac{a_1 z + b_1}{-a_2 z + b_2} \tag{2}$$

where R is the ratio of the two intensities I_1 and I_2. We can readily extract z from eq. (2). In our embodiment, the illumination is extended along the line-scan-array axis. We create the intensity gradient by using the light-to-dark transition regions at the edges of a focused beam, as we describe later. These gradients are well represented by a Gaussian equation.

To calibrate the system, a calibration plate

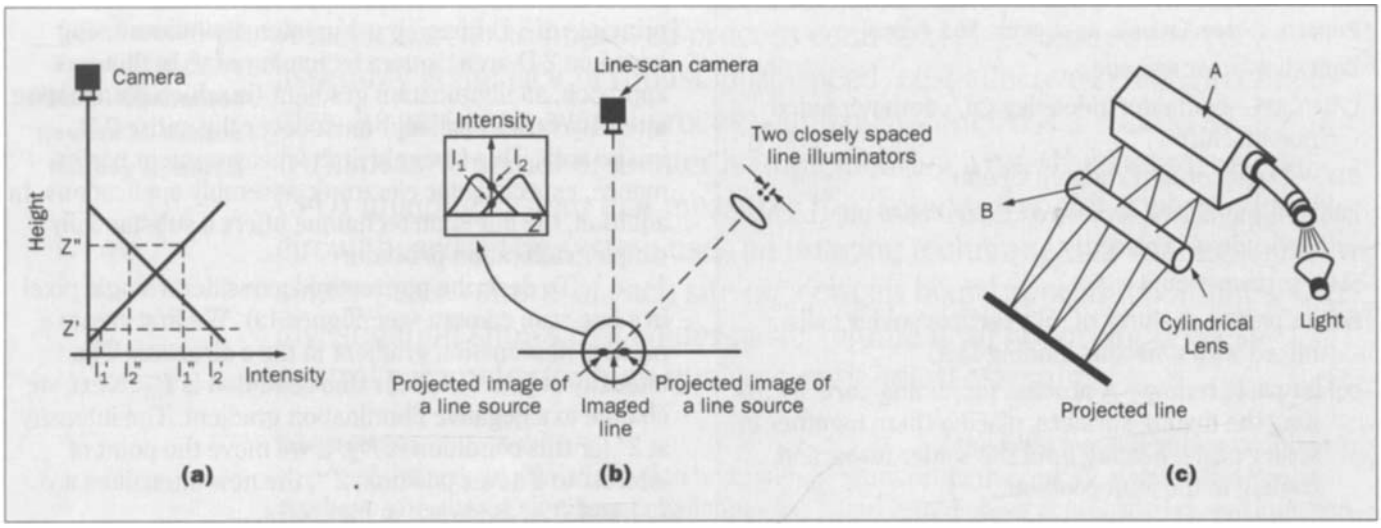


Figure 1. (a) Two linear intensity gradients and their respective intensities at height Z' and Z''. A unique ratio of intensities is created for every height (z), regardless of scene reflectance. (b) Basic configuration of the line-scan camera and the optical illumination system. (c) Light projection system with a single illuminator.

consisting of a precision ramp that spans the required z range is imaged twice with the two different illuminations. From these image data, we derive the coefficients of the Gaussian illumination profiles for each pixel. Using these calibration coefficients, we reconstruct 3-D scenes from pairs of 2-D images.

In Reference 5, we show that the accuracy of the height estimate depends on scene reflectance and the system noise level. As the scene reflectance, K, decreases, the relative error in height estimate increases and is proportional to $1/K$. The theoretical noise limit is determined by the digitization noise level of the camera system. For maximum reflectance, the maximum error in height estimate, N_z, does not exceed $1/2^{n+1}$, where 2^n is the dynamic range of the camera.[5] Our system employs a high-dynamic-range camera that digitizes its analog output into 4096 levels, giving $N_z \approx 10^{-4}$.

Experimental System Configuration

Figure 1b shows a basic configuration for the camera and optical illumination system. The two closely spaced illuminators can be switched on and off independently. In our system, we use a single light source, with two intensity gradients generated from opposite edges of the beam. This is achieved by moving the illumination system to an appropriate position prior to each of two image acquisition scans.

In the single-illuminator light projection system (shown in Figure 1c), part A of the light source consists of a circular bundle of optical fibers converted to a line in such a way that a quartz halogen light illuminating the bundle at the circle end produces a thin line of light at the other end. Part B is a cylindrical lens that projects and focuses the line source on the scene from which images are acquired. When the transition region is projected at an angle and positioned over the line viewed by the camera, it becomes our illumination gradient (see Figure 1b). We select angles and focusing parameters to maximize the z resolution for various scenes.

In this physical embodiment, the incident illumination angle will change slightly, possibly causing height measurement errors at particular points. These may occur on specular surfaces, where the reflectance changes rapidly with the incident illumination angle, violating our assumption (see eqs. 1 and 2) that reflectance is constant for both scans. An *a priori* knowledge of the characteristics of specular scenes generally allows us to choose illumination conditions that minimize this error. However, for less specular surfaces, such as solder paste, the effect is negligible.

Figures 2 through 4 are examples of images we obtained using this technique. Figure 2 shows four solder-paste deposits on a circuit board. The height of

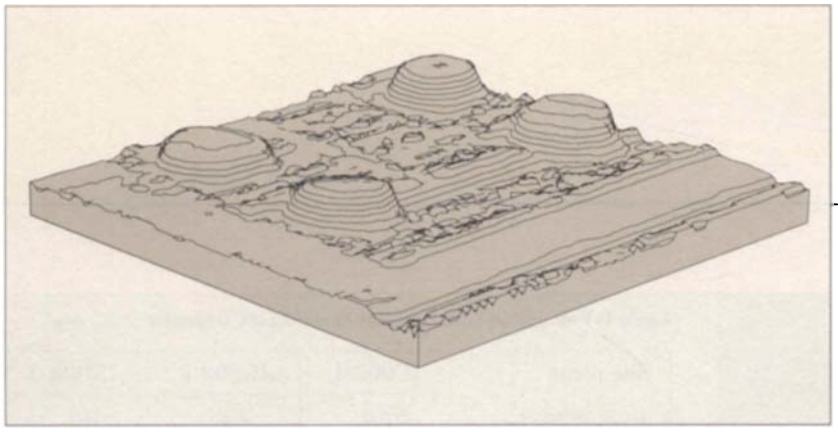


Figure 2. Four solder-paste deposits on a circuit board shown before SM components are in place. The deposits are about 10 mils high, and the field of view is 300 × 300 mils.

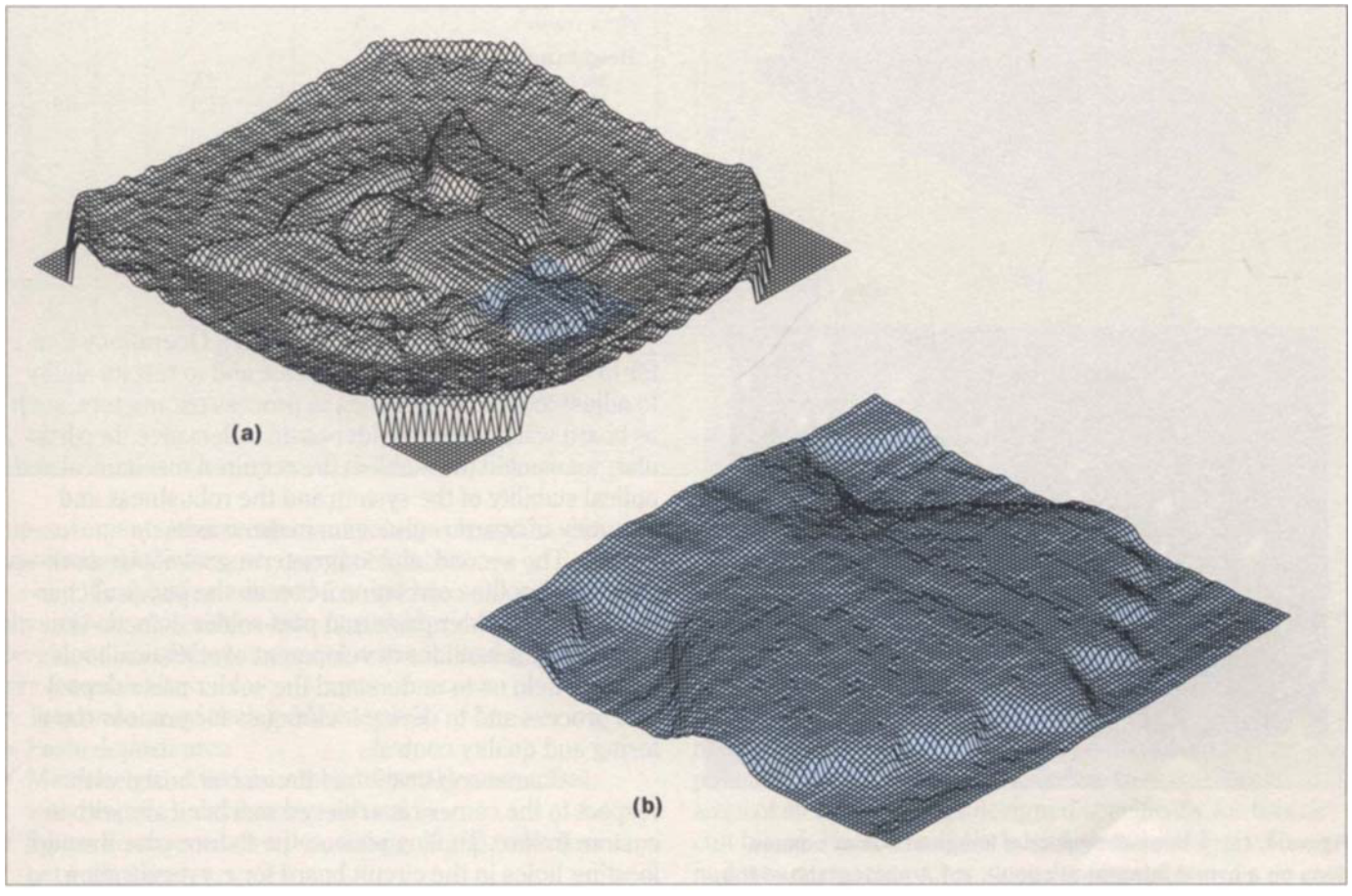


Figure 3. (a) Full 1" × 1" view of the topography of an eagle on a half-dollar coin, painted to minimize the effects of specularity. (b) A 200 × 200 mil section of (a) expanded to illustrate the detail.

the deposits is about 10 mils, and the field of view is 300 × 300 mils. Figure 3 shows the topography of an eagle on a half-dollar coin that was painted to minimize specularity effects. Figure 4 is a 3-D image of solder connections on a hybrid integrated circuit. Although some of these surfaces are highly specular, we chose illumination angles that minimized direct reflections.

For circuit-board assembly and process control applications, the field of view is large and the required resolution high. Normally, large volumes of data would have to be processed and stored. Fortunately, we were interested only in predefined regions on a board. To avoid processing and storing every pixel in the image, we designed a programmable camera interface. The program stored in the interface is derived from a computer-aided design/computer-aided manufacturing (CAD/CAM) database for the circuit board that is being scanned. The interface then operates as a switch, which writes image data to memory, just from predefined areas of interest. The performance advantages are twofold:

- The amount of memory required for a given

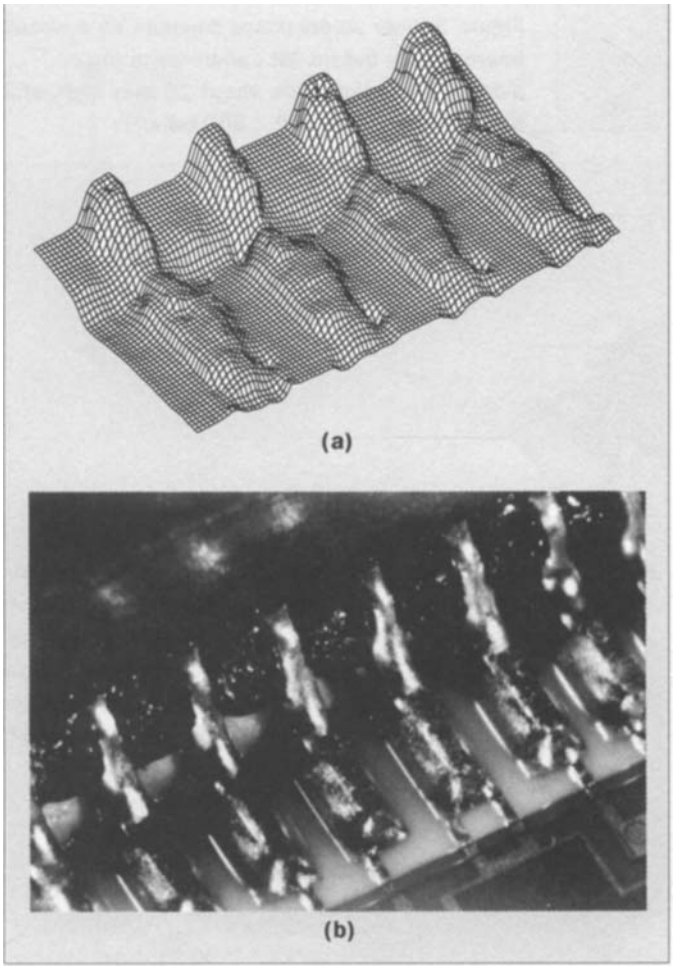


Figure 4. (a) A three-dimensional image of solder connections on a hybrid integrated circuit. (b) A photograph of the circuit shown in (a).

application is greatly reduced (in scanning a typical circuit board, only about 10 percent of the board's area contains image data of interest)

- Image processing can take place as the images are being acquired.

Solder-Paste Process Characterization

In our study of the solder-paste process, we set two goals: to test how well the 3-D imaging technique could measure solder-paste volume and to investigate the correlation between the physical characteristics of solder-paste and post-solder defects.

Table I. Production-Line Data for Three Paste Deposits

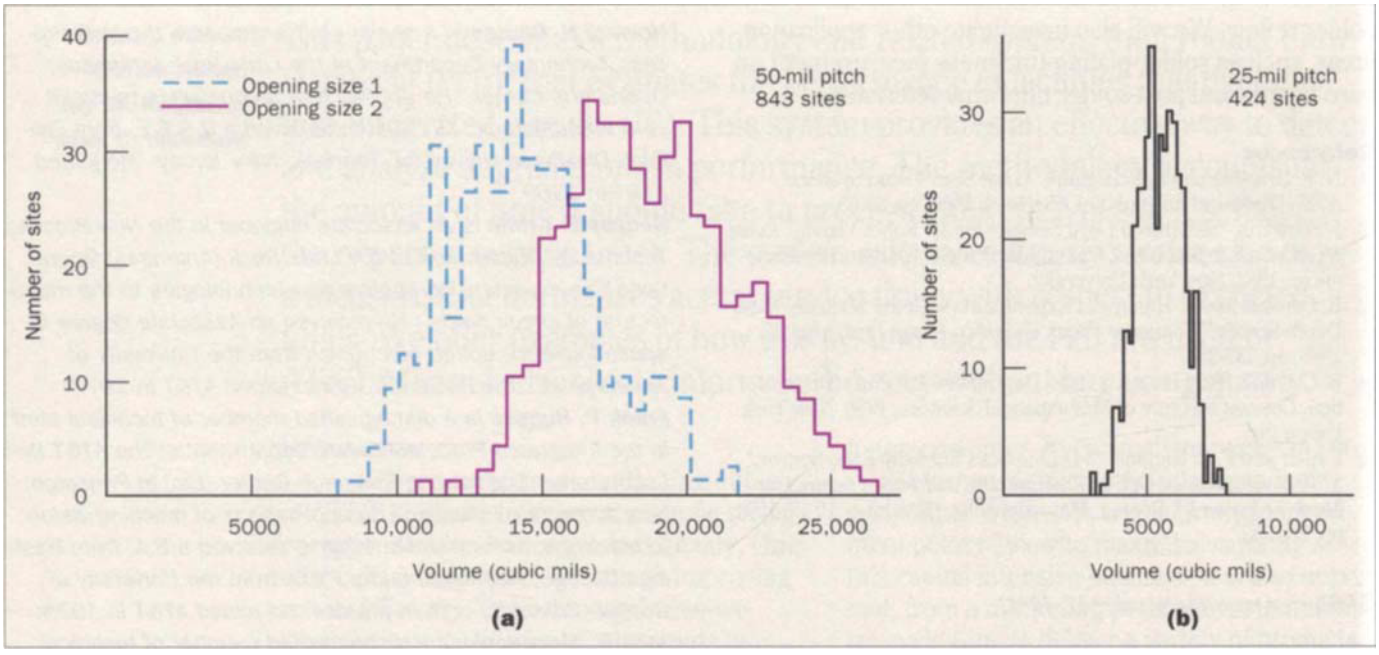
Site name	IC002-1	IC002-2	IC002-3
Total volume ($mils^3$)	5200	5620	66
Area ($mils^2$)	580	588	30
Height (mils)			
Mean	8.9	9.5	-
Maximum	12.0	11.0	4.0
Offset (mils)			
X	1	2	-
Y	2	3	-
Smear (percent)			
Right	35	25	-
Left	30	22	-

We used the AT&T Little Rock Operations Center to evaluate system performance and to test its ability to adjust to typical variations in process parameters, such as board warpage and solder-paste reflectance. In particular, we wanted to establish the required mechanical and optical stability of the system and the robustness and accuracy of board registration in three axes.

The second, and longer-term goal of our work—investigating the correlation between the physical characteristics of solder-paste and post-solder defects—is continuing. It includes development of statistical tools that will help us to understand the solder-paste deposition process and to devise techniques for process monitoring and quality control.

Coarse registration of the circuit board with respect to the camera is achieved mechanically with a custom fixture. Tooling pins on the fixture pass through locating holes in the circuit board for x,y registration. The fixture also positions the top surface of the board at a fixed z location on a vacuum plate. Repeatability is within a few mils in all three axes. The high z repeatability allows us to use the z dynamic range to maximize z resolution fully. We achieve fine x,y,z image registration by referencing CAD-defined circuit traces near each site.

We compared height measurements obtained from the 3-D imaging system with results obtained from a depth-measuring microscope. For smooth-paste topography, the results agreed well within 1 mil. With highly varying and irregular topography, individual point measurements were subject to noise from multiple reflections, but the average of the height measurements retained high precision. Because of the precision of the height



measurements, the accuracy of volume measurements was limited by system x,y pixel resolution.

For studies initiated to correlate solder-paste physical characteristics with post-solder defects, we developed algorithms to measure the following parameters for each site:

- Total volume of each solder deposit
- Paste deposit area
- Mean height, maximum height, and deposit offset with respect to land center in x and y
- Smear (measured as a percentage of gap reduction between sites).

Table I gives a sample of production-line data for three paste deposits. The last reading shows very low paste volume; post-reflow inspection confirmed that this site exhibited an *insufficient solder* fillet.

During the initial investigation, we collected data from dozens of boards representing a variety of board codes that typically held 1000 to 2000 sites per board. We visually inspected sites that had significant paste-volume deviations after reflow. All sites that had less than one-third of the nominal paste volume were rejected as exhibiting insufficient solder fillets after reflow. This initial correlation provides a strong incentive for future work that will include on-line statistical analysis to control the solder-paste-deposition process.

Figure 5. Solder-paste volume distribution from one board. (a) 50-mil-pitch component sites with two stencil-opening sizes. (b) 25-mil-pitch component sites, all with the same stencil-opening size.

Figure 5 shows the solder-paste volume distributions for one board that we analyzed. The paste-volume distribution of sites in Figure 5a had 50-mil pitch components. The two distributions relate to two different sizes of stencil openings designed specifically for this circuit board. Each 25-mil pitch land shown in Figure 5b had stencil openings that were the same size.

Summary and Future Work

We have described a new 3-D sensing technique and its initial application to the solder-paste deposition process. Even in this initial study, we have found that monitoring solder-paste volume can be a powerful predictor of solder-joint quality and should be an important tool for on-line process control. We are continuing to investigate the correlation between solder-paste volume and solder-joint quality.

Future applications of the 3-D system may include post-placement device lead registration in x,y and z (z lead registration is also referred to as lead coplanarity). These measurements can be made before or after

solder reflow. We will also investigate other application areas, such as solder-plating-thickness measurement on bare boards and post-solder fillet characteristics.

References

1. N. R. Brunelle and F. P. Higgins, "Line Scan Vision System," *AT&T Technical Journal*, Vol. 65, No. 4, 1986, pp. 58-65.
2. J. Schwartz, "Structured Light Sensors for 3D Robot Vision," *Robotics Research Report No. 8*, Courant Institute of Mathematical Sciences, 1983, New York University.
3. B. Carrihill and R. Hummel, "Experiments with the Intensity Ratio Depth Sensor," *Computer Vision Graphics, Image Processing 32*, 1985, pp. 337-358.
4. B. Carrihill, "The Intensity Ratio Depth Sensor," Ph.D. Dissertation, Courant Institute of Mathematical Sciences, 1986, New York University.
5. I. Amir and F. P. Higgins, "3-D Line-Scan Intensity Ratio Sensor," *SPIE Symposium on Optics, Illumination, and Image Sensing for Machine Vision VI*, Boston, Massachusetts, November 10-15, 1991, pp. 240-252.

(Manuscript received December 17, 1991)

Israel Amir *is a member of technical staff in the Integrated Process Control Department at the AT&T Bell Laboratories Engineering Research Center (ERC) in Princeton, New Jersey. He is currently working on machine vision for process control. Mr. Amir received a B.S. in electrical engineering from the Technion, Haifa, Israel; an M.S. in electrical engineering from Purdue University, West Lafayette, Indiana; and a Ph.D. in electrical and computer engineering from Drexel University, Philadelphia, Pennsylvania. He joined AT&T in 1985.*

Howard N. Gaston *is a senior staff engineer in the New Process Technology Department at the Little Rock (Arkansas) Operations Center. He applies new technologies to circuit card manufacture. Mr. Gaston received a B.S.E.E. from Fairleigh Dickinson University, Teaneck, New Jersey. He joined AT&T in 1969.*

Rodney E. Griffin *is an associate engineer in the New Process Technology Department at the Little Rock (Arkansas) Operations Center, where he applies new technologies to the manufacture of circuit cards. He received an Associate degree in applied science united electronics from the University of Arkansas at Little Rock. Mr. Griffin joined AT&T in 1977.*

Frank P. Higgins *is a distinguished member of technical staff in the Integrated Process Control Department at the AT&T Bell Laboratories Engineering Research Center (ERC) in Princeton, New Jersey. He is working on applications of machine vision to electronic assembly. Mr. Higgins received a B.A. from Hastings College, Nebraska, and a Ph.D. from the University of Denver, Colorado, both in physics. He joined AT&T in 1978.*

John B. Macdonald *is a distinguished member of technical staff in the Machine Vision Department at the AT&T Bell Laboratories Engineering Research Center (ERC) in Princeton, New Jersey. He works on machine vision hardware and software design CAD processing and information displays. Mr. Macdonald joined AT&T in 1968, after receiving an M.A. in physics and electrical engineering at Cambridge University, United Kingdom.*