International Mandatory Product Standards

Donald N. Heirman
Steven M. Crosby
Douglas C. Smith

Competing for global markets requires compliance with mandatory standards as a critical aspect of the product realization process. The extent to which the product team is aware of product standards is reflected in its ability to move the product through the design specification, development, and testing phases of product realization. Recent developments in regions such as the European Community and the Pacific Rim have created the need for increased awareness of present and proposed international mandatory product standards. This paper presents the projected evolution of these standards, and some practical design implementation strategies are offered at both the system and printed wiring board levels.

Introduction

For corporations to remain profitable in globally competitive markets, all aspects of bringing a product to market must be carefully planned, and each phase must be optimized. A corporation cannot remain profitable unless it methodically pursues mandatory product standards.

Gradually gathering compliant design standards information with each design iteration is now a thing of the past. Rapid increases in technology are shrinking the average market window for a product. This implies that product development schedules and costs must be minimized by making the primary design consideration have built-in quality systems that emphasize compliance with mandatory product standards.

Optimizing Communications

Effective communications between and among project team members are crucial when entering new markets with unfamiliar regulation. AT&T, in its effort to expand the market boundaries for new products, must gather information about all mandatory standards that apply to its products. In dealing with multinational markets, a product design may require a modular approach that will address the differences in the product's anticipated operating environments.

The concept of designing for multinational products must extend beyond dealing with differences between power sources and telecommunications networks. It also must accommodate a composite of the mandatory standards for the multinational product. To simplify the design approach, a worst-case composite must be created for all mandatory design requirements such as tip-ring spacing dimensions for voltage breakdown tests, and the various regulated emission and immunity levels spanning the frequency spectrum. This composite will also reflect multiple distances between test equipment and the equipment under test (in the case of radiated emission measurements), and will specify the equipment under test configuration that is required.

Electromagnetic compatibility (EMC) and product safety considerations affect a product's physical design attributes. Not communicating these requirements will result in the prohibitive cost penalties associated with hardware redesign. The team, once expecting record profits, will now be struggling simply to break even.

The International Directives

Internationally marketed products must meet a growing array of mandatory standards. Conformity assessment (CA) combines product design type approval, conformance testing to mandatory standards, test lab

Panel 1. Acronyms in This Paper

ANSI — American National Standards Institute
CA — conformity assessment
CAD — computer aided design
CB — Competent Bodies
CENELEC — European Organization for Electro- technical Standardization
CISPR — Special International Committee on Radio Interference
CTR — Common Technical Regulation
CW — continuous wave
DSR — double-sided rigid boards
EFT — electrical fast transient
EMC — electromagnetic compatibility
EMI — electromagnetic interference
ESD — electrostatic discharge
EC — European Community
FCC — Federal Communications Commission
IEC — International Electrotechnical Commission
ISDN — Integrated Services Digital Network
ISN — impedance stabilization network
ISO — International Standards Organization
ITE — Information Technology Equipment
LAN — local area network
MLB — multi-layer board
NB — Notified Body
PSTN — public switched telephone network
PWB — printed wiring board
QS — quality system
RF — radio frequency
TCF — technical construction file
TTE — Telecom Terminal Equipment Directive

accreditation, and quality system registration. Proof of compliance with these standards is a major ingredient of conformity assessment. Though mandatory standards are proliferating in the areas controlling radio frequency (RF) emissions and immunity of products, throughout the world the European Community essential requirements in EMC continue to lead this standards activity. These CISPR emissions requirements have been adopted by the European Organization for Electrotechnical Standardization (CENELEC) and are called European Norm EN55022. It is effectively a copy of CISPR Publication 22. To ensure a comprehensive set of standards and procedures to improve future marketing, design, manufacturing, and testing practices, AT&T is actively working both with international standards organizations and other forces influencing EMC and product safety standards-setting. Many of these activities directly affect norms being written and published for the European Community (EC).

One additional conducted emission requirement has been proposed for the revision of CISPR Publication 22. The revised requirements will be applied to telecommunications product signal ports connected to both unshielded and shielded twisted conductor pairs. A typical application would be in products connected to the public switched telephone network (PSTN) and to extended local area networks (LANs) such as Ethernet or Token Ring. Table I shows proposed signal ports limits for Class A equipment.[5] Recent work to develop an impedance stabilization network (ISN) test setup for measuring conductive emissions for both shielded and unshielded twisted pair cabling has been introduced.

EC Standards Effect on U.S. Standards

Our earlier paper in the *AT&T Technical Journal*[1] (see Figures 1 and 2 in that paper) notes that the RF emission limits of the International Electrotechnical Commission (IEC) Special International Committee on Radio Interference (CISPR) Publication 22[2] are more severe than similar limits set by the U. S. Federal Communications Commission (FCC). [Note that above 960 Megahertz (MHz), the limit for the FCC Class B curve in Figure 3 of our cited work should be 44 decibels (dB) above a microvolt per meter, not 39 dB as shown.]

There is a dramatic impact on product design from having to reduce conducted power line emission limits down to 150 kilohertz (kHz). This is because the harmonics of switching power supplies now have additional requirements between 150 and 450 kHz (the lower frequency limit for the FCC regulations). Between 88 and 230 MHz, the CENELEC/CISPR limits are 4 to 6 dBs more restrictive. With significant product clock frequency harmonics in that frequency band and with substantive differences with respect to the FCC limit, there is a real potential for design rework or need for external

Table I. Proposed CISPR Publication 22 Signal Port Conducted Emission Limits
Limits of conducted common-mode (asymmetric mode) disturbances at Telecom ports in the frequency range 0.15 MHz to 30 MHz for Class A equipment.

Frequency range MHz	Voltage Limits [dB(μV)]		Current Limits [dB(μA)]	
	Quasi-peak	Average	Quasi-peak	Average
0.15 to 0.5	97 to 87	84 to 74	53 to 43	40 to 30
0.5 to 30	87	74	43	30

The lower limits shall apply at the transition frequency.

Note: The limits decrease linearly with the logarithm of the frequency in the range between 0.15 MHz and 0.5 MHz. The current and voltage disturbance limits are derived for use with an Impedance Stabilization Network (ISN) which presents a common-mode (asymmetric mode) impedance of 150 ohms to the signal port under test (conversion factor is $20 \log_{10} 150\ (\Omega) = 44\ dB\Omega$).

suppression to meet these new limits.

The FCC has released a Notice of Proposed Rule Making on adopting CISPR Publication 22 to replace the digital device limits in Part 15 of their Rules and Regulations. MP-4 is the FCC's measurement method corresponding to that in CISPR Publication 22.[3] This proposal asks U.S. industry if it prefers one international harmonized standard, or whether manufacturers should have a choice of either the FCC Part 15 Rules and measurement procedures, or those contained in CISPR Publication 22. Final action by the FCC is expected by the end of 1993, at which time the next edition of Publication 22 is expected.

MP-4 will be replaced by ANSI C63.4-1991[4] by May 1, 1994. During the transition either MP-4 or C63.4-1991 can be used. The proposed amendment to the next edition of CISPR Publication 22 (which probably will not occur until 1994) will be closer to ANSI C63.4-1991. Hence, harmonization appears almost assured between the FCC digital device measurement practice and the practice to be presented in the amended Publication 22.

Immunity Standards

The emphasis for product immunity in the EC EMC Directive differs greatly from the voluntary immunity emphasis in the United States, where the FCC does not regulate digital device [Information Technology Equipment (ITE)] immunity.[1] U.S. manufacturers now determine on their own how much immunity is adequate. In the EC, a set of generic immunity standards—EN 50082-1—was published in April 1992 in the Official Journal of the European Communities.[6] It provides limits and methods to measure immunity outlined in Table II, and hence a harmonized standard that must be met before the CE Mark can be applied to the product to allow free flow with the 12 EC member states.

The generic standard applies if product-specific standards do not exist, i.e., no standard applies to such equipment as ITE. CISPR has a working group developing ITE immunity standards that will take precedence over the generic standard. This standards proposal (currently identified as CISPR Publication 24) also has been introduced into the EC standards setting body CENELEC to assure international harmonization.

At the time of this writing, no surge (e.g., lightning) or conducted immunity tests were identified in the generic standard, although these tests are well on the way to becoming required because they are now part of the informative annex of the generic standard. Informative annexes become part of the normative standard when the basic methods of measurement standards are published, and the EC recognizes the changes of status.

Conforming to the EMC Directive

The EMC Directive was enacted in 1989.[7] The directive states that products must meet essential EMC emission and immunity requirements. A transition period was announced in April 1992 that makes it effective December 31, 1995.[8]

The EMC Directive applies to a broad range of products, especially ITE products, including telephone networks and apparatus. We will later discuss the basics of the Telecom Terminal Equipment (TTE) Directive[9] that went into effect in November 1992, and that takes precedence for equipment attached to the PSTN. Manufacturers are awaiting the mandatory technical requirements that are being drafted. This paper will concentrate

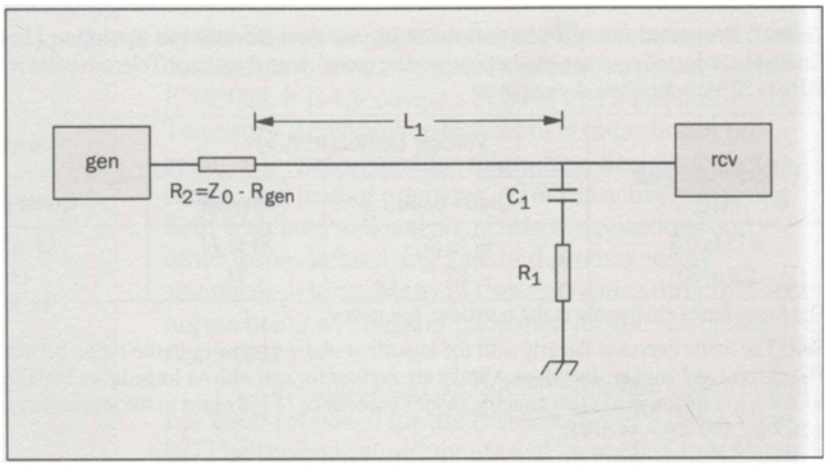

Figure 1. The correct distribution of a clock signal. Typical values for the components are: R2=Zo - Rgen where Zo is the characteristic impedance of the path on the board and Rgen is the output resistance of the clock driver, C1=100 picofarads (pF), and R1=100 to 200 ohms for some popular logic families. L1 is the length of the line delivering the clock signal.

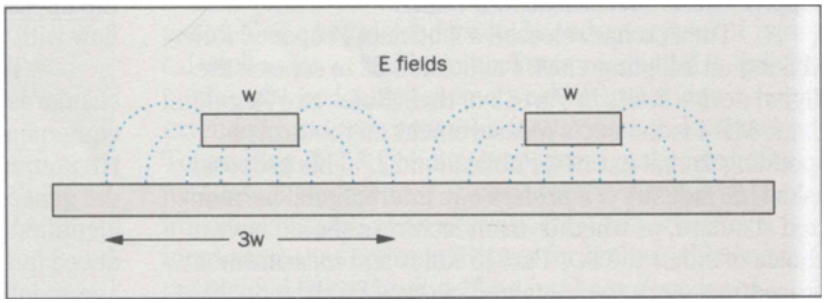

Figure 2. The configuration of two 50 ohm striplines, i.e., transmission lines formed over a ground plane. The E-fields from the signal conductors cover a width 3 times that of the conductor. Beyond that distance, the field strengths are low enough to be negligible.

on discussing the EMC directive that can be used now to gain access to the EC for products other than those connected to the PSTN that still require country-by-country type approvals.

Manufacturers' voluntary declarations of conformity to the EMC Directive are highly desirable. The Directive states that such declarations can be made for equipment other than that covered by other directives (e.g., the TTE Directive), and radio transmission products.

The Declaration of Conformity contains the following:

- Product description
- Specification reference and any national measures to ensure conformity
- Signatory empowered to bind manufacturer or authorized representative in the EC
- References to EC type-examination for such products designed for radio communication. (This is not applicable for voluntary declaration.)

For example, the manufacturer or an independent test lab would run tests on a product to meet the emission and immunity essential requirements. The manufacturer keeps the test report, declares conformity, and applies the CE mark (see below). The Declaration of Conformity is described in Annex I of the EMC Directive.

Because the Declaration of Conformity also applies to the higher controlled directives, reference must be made to any EC-type examination certificate for such products such as those covered by the TTE Directive. These certificates are provided by Notified Bodies (NBs) that also are held to strict criteria contained in the TTE Directive. Except for items associated with administering the higher-controlled Directive, the Panel 2 criteria also largely apply to Competent Bodies (CBs), i.e., testing organizations or agencies appointed by a national government in the EC to administer a specific EC Directive.

Thus, NBs play a role similar to the FCC's in administering ITE products needing certification, e.g., personal computers (PCs) and their peripheral devices. Hence, NBs are formally "notified" to the European Commission by the national government under specific directives.

Another possibility for showing conformance to the EMC directive is to use a technical construction file (TCF). This approach is spelled out in the EC EMC

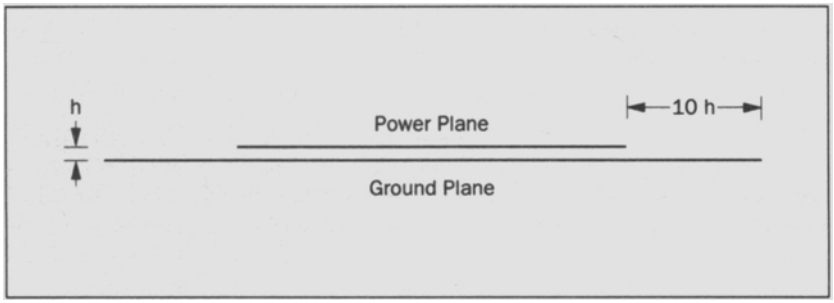

Figure 3. The magnetic field fringing effects between the power and ground planes of a multilayer PWB, here configured so the copper plane edges do not overlap. The point is to capture the loose flux at the edge of the planes and thereby reduce the product's high frequency emission characteristics.

Directive in Article 10.2. It can be used when harmonized standards do not exist, or when there are reasons to not apply them. The TCF route currently is available to products not designed to transmit radio communications and not connected to the public switched telecom network (EMC Directive, article 10.5). Briefly stated, a typical TCF contains the following:

- Description of product or apparatus
- Procedures used to ensure conformity with the essential requirements of the Directive
- Technical report or certificate from a Competent Body.

The TCF must be available to the Competent Body for 10 years after the product goes on the market.

CBs are specifically required to administer and approve TCFs. In some EC countries there are multiple CBs, while in others there may be one or may use another EC country's CB rather than establish their own.

The TCF can also be used for conformance within a family of products with smaller differences, e.g., features sets. For example, a telecom transmission frame with many plug-in cards, operating from the same backplane and power supply, can be assessed as a *family conformance* by measuring a worst-case combination of these plug-ins from an emission and immunity perspective. All combinations need not be measured. A CB could approve the rationale for such combinations while the tests are being performed by the CB or the CB-approved manufacturer's or third party's test organization.

The CE Mark

The CE Mark is a product conformity mark consisting of the letters CE and the year it is affixed to the product. The CE Mark shows that the product conforms to *all applicable* directives. This means that one mark can cover EMC, TTE, and (for example) future low-voltage safety directives. When an EC-type examination certificate is issued by a NB, the CE mark must be accompanied by the NB's distinctive letters or numbering scheme. Both the year and number/letter requirements will be governed by the proposed CE marking directive of 7 December 1992. Until this directive is in place, the language about the CE marking in the EMC Directive remains in use, to be superseded by the CE marking directive. Whether the NB number and date will appear next to the CE marking is still being debated.

Harmonization of standards and labeling across the EC is ultimately good for manufacturers to avoid multiple labeling of products. However, the differing transition periods for implementing each EC directive complicate the testing and labeling plans for each product.

It must be noted that the CE Mark is for use by national market inspectors, not consumers. It is not a quality, safety, or environmental protection mark. It can be affixed to each product and/or the packaging material, user's manual, or warranty certificate. The EC expects end-users to prefer products bearing the CE Mark, and to report violations. The product itself must be marked if possible.

When the CE Mark must be affixed depends on when products are considered placed on the EC Market. "Placing on the market" means first making available against payment or even free of charge to a user.

The mark covers the following types of products:

- New products manufactured in the EC, or new or used products imported into the EC
- Products sold to a customer
- Products offered via a distribution chain
- Products imported directly for the EC manufacturer's own use.

The mark does *not* apply to the following:

- Manufacturers providing products to a party responsible for meeting the EMC Directive
- Products re-exported out of Europe by EC importers
- Products exported out of the EC
- Products displayed at trade fairs and exhibitions.

Table II. Generic Immunity Standard Categories, EN 50082-1:1992

Electrostatic Discharge	(8 kV air discharge)
Radiated Electric Field	(3 V/m unmodulated between 27 and 500 MHz)
Fast Transients/Common Mode (applied to signal and control lines whose total length may exceed 3 meters)	(0.5 kV, 5 nanosecond rise time, 50 nanosecond impulse duration at a 5 kHz repetition rate)

Routes to Compliance with the EMC Directive

Four compliance routes exist:

- Applying harmonized CENELEC Standards (Article 10.1 of Reference 7).
- Preparing a Technical Construction File (Article 10.2 of Reference 7).
- For radio-communication transmission equipment and telecom terminal equipment, an EC-type examination (Article 10.5 of Reference 7). See the following section on the TTE Directive for details.
- Applying present EC member state national standards.

When harmonized standards are applied, a manufacturer's self-declaration of conformity must be certified by an EC Declaration of Conformity issued by the manufacturer or its authorized representative established in the EC. For all practical purposes, Module A of Reference 10 is applied during the design phase when the manufacturer prepares the technical design documentation. It is kept available for review by the national authorities in the EC.

During first production, the manufacturer declares conformity with the EMC Directive's requirements on emission and immunity, and then affixes the CE Mark. Though this route is most attractive because the manufacturer retains control, it has the potential for the most challenge within the EC.

The TTE Directive

The TTE Directive[9] applies to telephone equipment that directly or indirectly [e.g., a phone behind a private branch exchange (PBX)] connects to the PSTN. It does not include most network and central office equipment that is covered by the EMC Directive. Computers are considered terminal equipment via their connection to the PSTN. But the directive would apply specifically to the modem or interconnect component, not to the entire computer. Because a modem card cannot operate apart from the computer, it obviously would have to be included in a test setup for emission and immunity EMC tests.

Determining conformance to the TTE Directive requires testing to harmonized European standards. These standards will be identified in a series of Common Technical Regulations (CTRs) being written primarily for digital services including the ISDN (Integrated Services Digital Network) and various data protocols such X.21 and X.25. These CTRs treat as essential the EMC requirements related to the TTE, harms to the network, effective use of the radio frequency spectrum, interworking with the PSTN, and interworking of TTE via the PSTN. The requirements for product and public telecommunication network operator safety not covered by the European low voltage directive[11] will not be covered by the CTRs, but will be met by conformance with other harmonized standards, i.e., the low voltage directive or other acceptable solutions justified by the manufacturer. A Notified Body will check this aspect.

Annexes of the TTE Directive offer a choice among procedures for assessing conformity to the applicable technical standards harmonized across Europe, the CRTs. These conformity assessment (CA) procedures are based on the 13 December 1990 EC decision[10] that specifies the selection of CA modules. CA can be established by:

- *Conformity to type* (TTE Annexes I plus II; Modules B plus C). The product is tested by a third party approved to do this kind of "type examination." This party is called a Notified Body (NB) indentified in TTE Directive Annex II. Continuing "conformity to type" of the manufactured product has to be shown by random product checks by the Notified Body.
- *Production Quality Assurance* (TTE Annexes I plus III; Modules B plus D). Product type-examination by the NB is the same as in the preceding example. Instead of "conformity to type," the production quality system must conform to EN Standard 29002 (same as ISO 9002).[12] The Notified Body for TTE is responsible

Panel 2. Minimum Criteria When Designating Notified Bodies

- The Notified Body, its director, and the staff responsible for carrying out the tasks for which the Notified Body has been designated, shall not be a designer, manufacturer, supplier or installer of terminal equipment, or a network operator or a service provider, nor the authorized representative of any of such parties. They shall not become directly involved in the design, construction, marketing or maintenance of terminal equipment, nor represent the parties engaged in these activities. This does not preclude the possibility of exchanges of technical information between the manufacturer and the Notified Body.
- The Notified Body and its staff must carry out the tasks for which the Notified Body has been designated with the highest degree of professional integrity and technical competence and must be free from all pressures and inducements, particularly financial, which might influence their judgment or the results of any inspection, especially from persons or groups of persons with an interest in such results.
- The Notified Body must have at its disposal the necessary staff and facilities to enable it to perform properly the administrative and technical work associated with the tasks for which it has been designated.
- The staff responsible for inspections must have:
  — Sound technical and professional training.
  — Satisfactory knowledge of the requirements of the tests or inspections that are carried out and adequate experience of such tests or inspections,
  — The ability to draw up the certificates, records and reports required to authenticate the performance of the inspections.
- The impartiality of inspection staff must be guaranteed. Their remuneration must not depend on the number of tests or inspections carried out nor on the results of such inspections.
- The Notified Body must take out liability insurance unless its liability is assumed by the State in accordance with national law, or the Member State itself is directly responsible.
- The staff of the Notified Body is bound to observe professional secrecy with regard to all information gained in carrying out its tasks (except vis-a-vis the competent administrative authorities of the State in which its activities are carried out) under this Directive or any provision of national law giving effect thereto.

for quality system (QS) conformity, even if another agency performs the assessment and surveillance under the aegis of the Notified Body. This ongoing QS surveillance eliminates the cost and time for the random product checks required by the conformity to type procedure above. Its downside is that the QA conformity has to be registered by a registrar accredited in the EC.

- *Full Quality Assurance* (TTE Annex IV, Module H). Here the manufacturer is entitled to self-declare conformity with the applicable standards because its QS conforms to EN Standard 29001 (same as ISO 9001).[13] covering both product design and production. Here too the NB for TTE is responsible for QS approval and surveillance, even if it is done by another agency accredited in the EC. The procedure is most cost-effective because it requires neither third party product testing nor random product checks.

This material should suggest that it is critical for telecommunications product manufacturers to keep abreast of the impact not only of the EMC Directive but also to the TTE Directive and its associated ISO quality standards 9001 and 9002. In selected a Notified Body for the Production Quality Assurance and Full Quality Assurance procedures, it is essential to establish the working relationship between that NB and the QS registrar up front to assure that only one of these third parties assesses conformity and conducts surveillance to ISO 9000 standards.

We now turn to the practical design steps to meet the most onerous of the international and EN essential requirements, i.e., designing the product to work in an RF steady-state and transient environment. This process is called *RF immunization* or product *RF immunity.*

Designing for RF Immunity

The importance of designing for RF immunity to the expected electromagnetic environment is important not only for equipment reliability, but also legally and contractually, because customers and some governments have mandated equipment performance in this area. Furthermore, the emphasis on quality awareness has

increased the demand for equipment that functions properly in its intended RF environment. This can happen only when the equipment has appropriate levels of RF immunity to electromagnetic interference (EMI). This section briefly covers some concepts related to designing for RF immunity.

RF immunity requirements have traditionally been specified in two ways:

- For continuous wave (CW), amplitude modulated, radio frequency conducted and radiated signals
- For pulsed EMI conducted and radiated sources.

The former category is meant to simulate the interference generated by radio transmitters; the latter deals with sources such as electrostatic discharge (ESD), electrical fast transient (EFT),[14] and surge that represent impulsive forms of interference.

This section will concentrate on tests for pulsed EMI because its requirements place the greatest stress on modern digital circuits. Circuits immune to pulsed EMI generally also will provide good immunity to amplitude modulated CW sources. This is especially true of equipment using digital technology.

The EMI Environment

Pulsed EMI can generate extreme levels of interference. For example, consider the induced voltage drop across a centimeter of wire with 10 nanohenries of inductance caused by an ESD-generated current that rises to 1 ampere in 1 nanosecond (ns). The voltage drop is given by L(di/dt)—i.e., the inductance L times the time rate of changes of current—or 10 volts per centimeter. The interference potential of this current is high. To make matters worse, 10 volts/cm is small compared to the possible values generated by ESD. Compared to other types of noise, digital logic noise can reach an L(di/dt) drop of 0.5 volt per centimeter, switching supply common-mode noise can reach 2 volts per centimeter, and a few volts per meter CW field will induce less than a few tens of millivolts per centimeter in a wire.

CW emissions can be a problem for the high field-strengths associated with small portable transmitters such as cellular phones that can be located inches from equipment. For this extreme case, techniques similar to those outlined below for pulsed EMI should be used.

Changing electric fields associated with pulsed EMI events can produce large parasitic currents. Take, for example, a change in voltage of 1 killivolt (kV) across 1 picofarad (pF) of capacitance in 1 ns. The current in the capacitor is given by C(dv/dt)—i.e., the capacitance times, the time rate of change of voltage—and is 1 ampere.

These two examples highlight parasitic coupling's potential to interfere with equipment. Therefore, good design practice must be followed if equipment is to exhibit immunity to pulsed EMI that provide high voltage and current levels in circuits for up to 50 ns.

Design Techniques

Design techniques can divert interference from sensitive circuits, and harden those circuits against the interference that reaches them. The techniques can be classified according to the frequency ranges.

Pulsed EMI is a broadband form of interference. The bandwidth of the available energy is a function of the type of pulsed EMI as well as the coupling modes. ESD can contain energy to beyond 1 gigahertz (GHz), whereas EFT is generally bandlimited to a few hundred MHz, and surge is limited to a bandwidth of only a few MHz. Design techniques that cover the ranges below and above 200 MHz are discussed in the next section. These techniques are effective for ESD and EFT.

Because structures that are good emitters are also generally good receiving antennas, the design techniques are similar to those that prevent unwanted emissions from high speed circuits. The difference between design for emissions and design for immunity is the particular circuits themselves, and leads to which the design techniques are applied. For instance, a 50 MHz clock lead would be an emissions problem, and high frequency design techniques would be used for such a signal. Techniques such as minimizing loop areas and path lengths on circuit boards are examples of what is required.[15,16] The 50 MHz clock would also be a concern for immunity, because a signal that changes states can be severely disrupted. Thus, high frequency design techniques help both emissions and immunity.

Consider the case of a reset lead. Such a signal would not likely be an emissions concern, but would surely be an immunity concern because a glitch on that lead would reset the system. Therefore the same high frequency design techniques would be applied to a reset lead to impart system immunity from pulsed EMI. The critical leads for immunity generally include those for emissions as well as additional ones, such as the reset lead.

Specific Techniques

This section discusses methods to work with frequency components below and above 200 MHz, and spark prevention in units using an insulating enclosure.

Frequency Components Below 200 MHz. Below 200 MHz, the effect of cables attached to products tends to dominate in conducting the interference into the product. The exception is direct ESD, where the spark injects current directly into the product. Provision must therefore be made to divert shield and cable currents induced by nearby pulsed EMI into the product before it enters the product's circuitry.

Design techniques for accomplishing the diversion of induced currents rely on skin effect and the free-space capacitance of the product's chassis. If the product has a metal enclosure, the skin effect will prevent EMI currents from reaching the circuitry by penetrating the enclosure except through holes and seams.[17] Also, if a cable shield is connected to the product's chassis, currents above a few MHz will flow from the cable into the chassis instead of penetrating the product. The chassis can thus be used as a free-space capacitor to remove high frequency energy from the cable shield.[18,19]

Ferrites also can be used to reduce common-mode currents from pulsed EMI on cables. This technique is especially useful when it is impractical to divert common-mode currents to a chassis. The ferrite used is a lossy material that can be modeled as an inductance in parallel with a 100 ohm resistor having an R-L corner frequency of a few tens of MHz.[20] Adding a ferrite to a cable can reduce common-mode current by as much as 50 percent, although the real amount is variable.

Cabinet or product enclosure issues—as opposed to cabling issues—generally become important above 200 MHz. Exceptions to this rule exist. One exception is a direct ESD to the enclosure and sensitive circuits still prevalent below 200 MHz.

Frequency Components Above 200 MHz. Above 200 MHz, product enclosure issues become important and even dominant. The dimensions of holes, seams, and slots in the enclosure can be comparable to a wavelength at these frequencies reducing the shielding effectiveness of the cabinet. A good compilation of guidelines is given in Boxleitner.[21]

Preventing the Spark. Some products, especially small portable types, use an insulating enclosure. For this equipment, the option exists to preventing direct ESD from affecting the product. Proper design of the enclosure to insure at least 2 to 3 centimeters (cm) of space between conductive system parts and charged objects, usually humans, is required [Boxleitner, pp. 40-41].

Summary of Immunity Concepts

Pulsed EMI and close radio transmitters can induce substantial interfering voltages and currents in electronic products. The amplitudes of voltages can reach up to hundreds of volts per centimeter induced on conductors through self and mutual inductance. Injected current amplitudes can reach amperes through only 1 pF of capacitance by electric field coupling. These transients can last up to 50 ns.

Special precautions must be taken to insure the product's immunity to this interference as legally mandated by many EC government authorities and by contractual requirements. Design techniques aim to divert interference away from sensitive circuits as well as to harden those circuits against the interference that reaches them.

Design Practices for High Speed Digital Circuits

There are several products with digital circuits and clock frequencies as fast as 1 GHz. Common- and differential-mode radiation from these circuits can make the product an unwanted source of interference. Furthermore, self-immunity becomes an issue because of interactions between high- and low-speed signals and circuitry. The printed wiring board (PWB) is still the most cost-effective way to accommodate EMC design techniques. However, it is only one element of the product, and the overall system design must be emphasized. Some EMC techniques we will address illustrate how the PWB, cable, and system enclosure components can interact electromagnetically, producing undesirable EMI characteristics.

The following sections recommend design techniques for high-speed digital circuitry that minimize the harmful effects of differential and common-mode radiation. These recommendations are by no means a cookbook solution to all PWB-level EMC design problems, but they are an excellent reference point from which individual circuit pack EMC solutions can be derived.

Clock Distribution Model

Figure 1 shows how a clock signal should be distributed. As illustrated, typical values for the components would be: R2 = Zo - Rgen (where Zo is the characteristic

impedance of the path on the board and Rgen is the output resistance of the clock driver), C1 = 100 pF, and R1 = 100 to 200 ohms for some popular logic families. The exact values depend on the logic family. L1 is the length of the line delivering the clock signal. If the clock signal is delivered to another point from the input of the first receiver (logic gate) in Figure 1, its length (L2) should be much smaller than L1, and will be short compared to the distance traveled by the signal during its rise or fall times. If these conditions are unmet, a separate distribution path similar to that in Figure 1 should go to additional receivers. This implies that a star pattern of clock distribution is preferable to a tapped bus arrangement.

Many types of resistors have an effective value that decreases above 400 MHz because of internal capacitance. By adding an appropriate ferrite bead in series with the resistor, almost constant resistance can be maintained to about a GHz. The ferrite must be selected so its inductive reactance is small compared to the value of the resistor at frequencies where the resistor still acts like a resistor. The ferrite must also show resistive impedance properties adequate to maintain the proper total resistance at higher frequencies where the resistor becomes less effective.

Lead and body inductances of the resistors can also be important. Lead length and resistor design should produce a small inductive reactance compared to the value of the resistor. Occasionally, a single resistor will have too much body inductance to work at the highest frequency of interest. Thus, several higher valued resistors whose parallel combination has the desired resistance could be used to lower the inductance of the total resistance at the expense of an increase in internal capacitance of the parallel combination of resistances. This technique is most likely necessary for resistors of a few tens of ohms that must work to frequencies above 100 MHz.

Minimizing the Effects of Differential Mode Emission

Every signal has a signal-return path, most often through signal ground. Reducing the area of the loop between these two portions of the desired signal will help minimize the effects of the radiating loop antenna formed by the physical orientation of the two paths relative to each other. The paths should be kept as short and close together as possible because emissions are proportional to the loop area and to the square of the frequency of the signals flowing in the signal/ground loops.

Emission levels are also proportional to the amount of high-frequency signal currents passing through conductors. In some circuit configurations, some currents may reflect backwards through the conductors. Therefore, efforts should be made to achieve the minimum current levels needed for circuit functionality. Maintaining uniform trace width and reducing trace discontinuities, such as the excessive use of vias and meandering paths, will improve the overall quality, performance and control of circuit interconnections, and will lessen circuit emissions at radio frequencies.

One frequently overlooked element of high speed digital design is the need to treat all high-frequency traces as transmission lines. Thus, designers should apply stripline or microstrip design technology for such signals.

Striplines are transmission lines formed over a ground plane. Figure 2, for example, shows the configuration of two 50 ohm striplines. The E-fields from the signal conductors cover a width 3 times the width of the conductor. Beyond that distance, the field strengths are low enough to be negligible. The result is that the fields extend one path width beyond the edge of the conductor. This implies that to minimize the effects of crosstalk, a 2W clearance should be maintained between these conductors (i.e., a center to center spacing of 3W). (Here *W* stands for the width of the conductor.) To autoroute these paths, temporarily set the path width intentionally wide for these conductors, autoroute them, and then return these paths to normal size W.

Traces carrying high frequencies are notorious EMI sources. Electric field radiations tend to concentrate around the sharp edges of conductors such as path corners. To avoid the E-field intensities associated with these sharp edges, circuit and PWB designers should avoid 90° cornering in high frequency traces on the PWB. Some computer aided design (CAD) systems offer rounded corners for high speed layouts, and almost all offer 45° routing capability.

Traces that connect to input/output connectors on the PWB should be impedance-matched. These input/output connections should then leave the PWB through coaxial cables or well-balanced twisted pairs. Cabling is always a critical aspect of a compliant design and, where possible, the cable length should be minimized.

Backplane traces are generally longer than those on PWBs. Unusually long parallel traces should have a

single properly matched impedance at the far end, and similarly long series traces should have a single matching impedance at their source. (Unusual length in this context means longer than the distance the signal travels during its rise or fall times, or length exceeding 1/10 wavelength for the highest frequency components of interest in the signal.)

When a PWB undergoes layout change activity, many thoughtful EMC compliance efforts often are compromised. Remember that when changing pathwork, the specified trace width and spacing must be preserved to maintain the proper impedance matching.

Minimizing the Effects of Common-Mode Emissions

The first step in reducing common-mode emission effects is to minimize interconnection lengths and insure a low impedance board ground. The PWB paths should be as short as possible, and layout guidelines should be assembled accordingly.

Trace width should be adjusted for proper control of impedance. All traces that carry high frequencies should be matched and terminated with the proper impedance. Impedance matching is 3-dimensional. Thus, the PWB design must show controlled impedance between board layers also.

Designing the power and ground layers of a multilayer PWB so the copper plane edges do not overlap will improve the magnetic field fringing effects between the power and ground planes (Figure 3). The point is to capture the loose flux at the edge of the planes similar to the 3W rule outlined above. This technique will reduce the product's high frequency emission characteristics.

The following information is relevant when deciding which plane edge—power or ground—to move inwards relative to the other plane. If the VCC layer has more common-mode noise than the ground layer, then it makes sense that the VCC layer plane edges should be moved inwards relative to the ground layer plane edges. Conversely, if the ground layer is noisier than VCC, then the ground plane edge should be moved inwards relative to the VCC plane edge.

Techniques for Minimizing Ground Noise

Despite the advantages of multi-layer board (MLB) technology, many cost-conscious product development teams still prefer double-sided rigid (DSR) boards. The changes, however, are the device technologies used on these DSR boards. DSR boards with fast switching components can easily exhibit ground noise difficulties because of voltages that appear across ground path inductances. The resulting unstable reference voltages can be an elusive source of false switching.

To minimize the effects of ground bounce[1] in DSR boards, the PWB designer should incorporate a tightly spaced power and ground grid. While EMC engineers have always claimed that any grid is better than none, some device technologies function more reliably when MLB technology is employed. Many manufacturers provide device application handbooks describing how to accommodate various board technologies. The Fairchild FAST Applications Handbook[22] is a reference of this type.

Multi-layer PWBs, with one or more layers dedicated for power and or ground, will lower the inductance (L) of the power and ground distribution system. Because the voltage swings that are attributable to ground noise are proportional to L [i.e., V=L(di/dt)], the stability of these reference voltage planes will improve over DSR PWB designs.

It is crucial to isolate high- and low-speed circuitry to avoid crosstalk, high frequency noise conduction, and their attendant emissions on low-frequency leads leaving the PWB. Sum-and-difference spurious frequencies may result from non-linear mixing effects on discrete frequencies in the circuitry. To prevent this, a separate VCC power plane can be employed to supply low speed circuits. This multiple power plane approach will improve the quality of signal flow while isolating the plans from noisy high speed circuits that are physically removed from quiet circuits. High speed power supply noise can be filtered from the PWB power supply connections by using bypass capacitors and ferrite beads. This technique suppresses such noise from appearing in the PWB power supply distribution system.

For some severe problems, shielding of high and low speed circuits may be needed. The use of case shielding should be supplemented on a PWB with grounded metallic covers (commonly known as a *can*) and flying fences, i.e, metal strips perpendicular to the board and connected periodically into the signal ground onto which the metal covers can be attached. These reflect high frequency energy away from quiet areas.

High frequency currents flowing in conducting material tend to concentrate near the surface. Skin depth in a conducting material is the depth where the

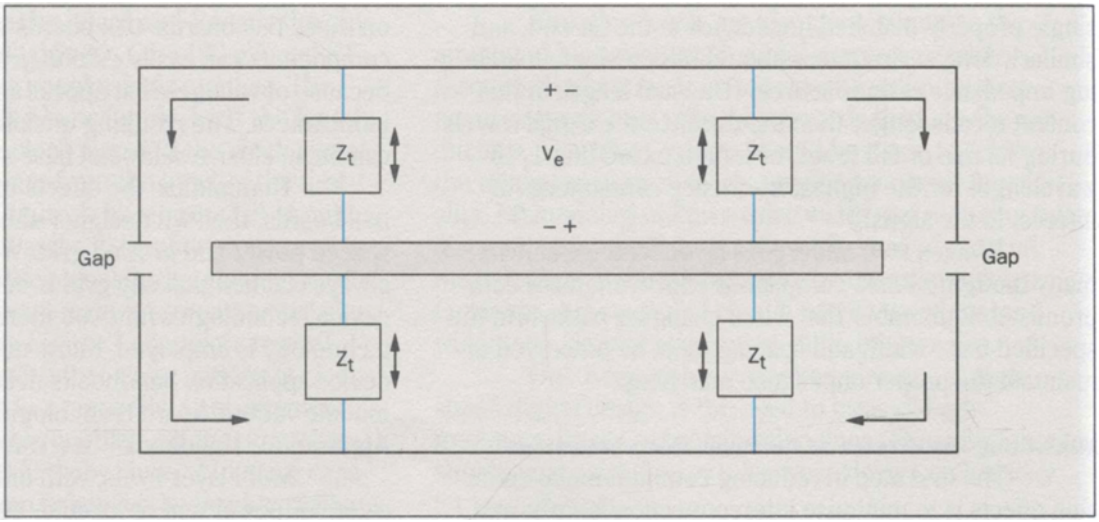

Figure 4. A PWB inside a conductive enclosure or cabinet. Capacitive coupling creates transfer impedances (Zt) between the PWB ground plane and the cabinet. These impedances combine with common-mode noise voltages on a PWB ground structure to produce current flowing between the board and the cabinet that cause eddy currents to circulate on the enclosure. When the eddy currents circulate around slots or gaps in the cabinet or enclosure, electric and magnetic fields will result.

current density has reduced to 37 percent or 1/e ("e" is the base of the natural logarithm) of the density at the surface. It is inversely proportional to the square root of the frequency, conductivity, and permeability of the conducting material. Most metals that can support their own weight are many skin depths thick at frequencies above a few MHz.

For covers and enclosures, use at least 3 skin depths of metal for a shield. At 10 MHz the skin depth of aluminum is 3 mils and for copper it is 1 mil. The material should require a low contact pressure where mechanical connections are required. Stainless steel, and conductive paints and coatings have serious shielding and mechanical reliability problems and should be avoided.

The design team can also use frame grounds to reduce common-mode emission. Multiple PWB frame grounds should be provided and, if possible, frame ground should be used as an outer PWB layer. This technique is especially useful in backplane designs.

System Level Noise Reduction Techniques

Approaching EMC compliance by considering the whole system versus only the subsystem, or system component level alone, will invariably lead to a more robust design in terms of product functionality, immunity, and compliance to mandatory product standards. Since no two systems are alike in terms of functionality and physical implementation, there can be no exact cookbook recipe for EMC compliance. Nonetheless, the following system level design techniques apply to many high frequency designs.

Consider the entire operating environment and configuration of the circuit when deciding the best EMC design implementation techniques for the given system. This means that the electromagnetic physical interactions among the system components—like a local shield on a PWB, the board itself, and the cabinet or enclosure—must be considered before deriving the subsystem component level solutions. This is especially true for designs with clock frequencies above 30 MHz and rise times faster than a nanosecond. A design of this nature will exhibit a power density spectrum with significant energy beyond one GHz.

Radiated Effects From Cabinet-Enclosed Circuitry

Envision a PWB inside a conductive enclosure or cabinet (Figure 4). Transfer Impedances (Zt) are created between the ground plane of the PWB and the cabinet via capacitive coupling. These transfer impedances combine

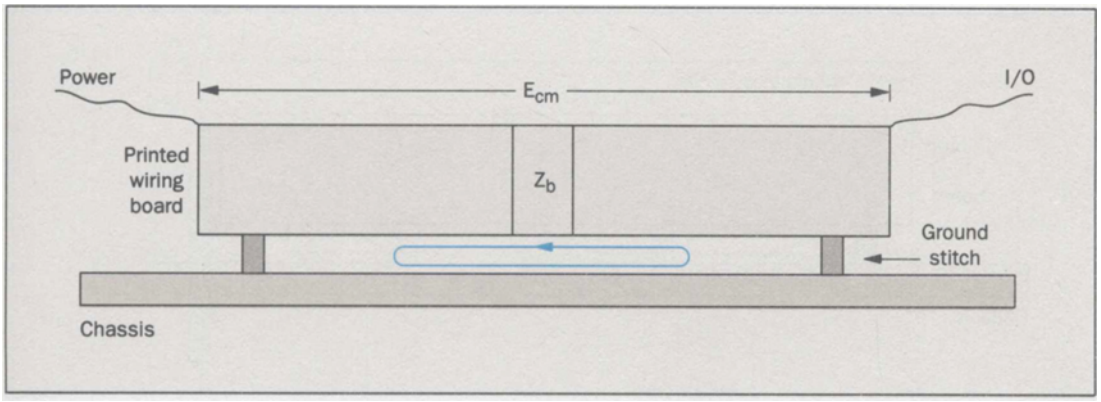

Figure 5. A board connected to a chassis by ground "stitches" to form ground "nulls" on the circuit board. Stitches are conductive connections from the PWB through a supporting member such as a mechanical stand-off, to the chassis itself and back to the PWB. This configuration is repeated both in and around the periphery of the circuitry to control the eddy current flow.

with common-mode noise voltages on a PWB ground structure to produce current flowing between the board and the cabinet that cause eddy currents to circulate on the enclosure. When the eddy currents circulate around slots or gaps in the cabinet or enclosure, electric and magnetic fields will result. RF currents can be induced on any cables running through or near these openings.

Electromagnetic induction of noise onto the cables can cause them to radiate at frequencies that can cause EMI problems to adjacent components or to nearby radio services. Suppose a 1"-square slot in a cable cabinet has a cutoff frequency of 400 MHz, the frequency below which a source of high frequency energy will be severely attenuated when trying to propagate through the slot. The smaller the slot the lower the attenuation. Induction onto a cable that passes near the slot can result in undesired cable radiation as low as 40 MHz. Most systems today have primary clock rates in the frequency range of this radiation. The following section details techniques to minimize these radiation effects by controlling where the eddy currents flow to minimize their effects.

Attaching the Printed Wiring Board to the Chassis

Figure 5 shows how a board may be connected to a chassis by ground "stitches" to form ground "nulls" on the circuit board. Here, *stitches* can be described as conductive connections from the PWB through a supporting member such as a mechanical stand-off, to the chassis itself and back to the PWB again. This configuration is repeated both in and around the periphery of the circuitry to control the eddy current flow.

The common-mode voltage across the board E_{cm} will drive leads coming off the board on opposite ends, e.g., a dipole antenna with power and input/output (I/O) leads. Stitching the board to the metal chassis in two places, causes a circulating current to flow through the board chassis and the stitches. This reduces E_{cm} thus shorting out the dipole antenna formed by the leads.

The circulating current causes a slot antenna to be formed. Enough stitches must be used to keep the size of this slot small relative to the wavelength of the frequencies generated on the board. High frequency components should also be grouped together with several close stitches enclosing the components. At each stitch, a common-mode "null" is created. A bypass capacitor of about 1000 pF should be connected from VCC to ground on the circuit board at each stitch.

Figure 6 illustrates a desired configuration for a board where the RF circuitry can be contained in a small area. Here, the stitches surrounding the RF circuitry cause local eddy currents to flow in the board, stitches, and chassis under the RF circuitry. However, the rest of the board is at ground potential, and an I/O lead exiting the right side of the board will not radiate significantly.

Emission from an Enclosure with Circuit Packs

Adding a shielded cable at the right side of the circuit board in Figure 7a, with the shield attached to the

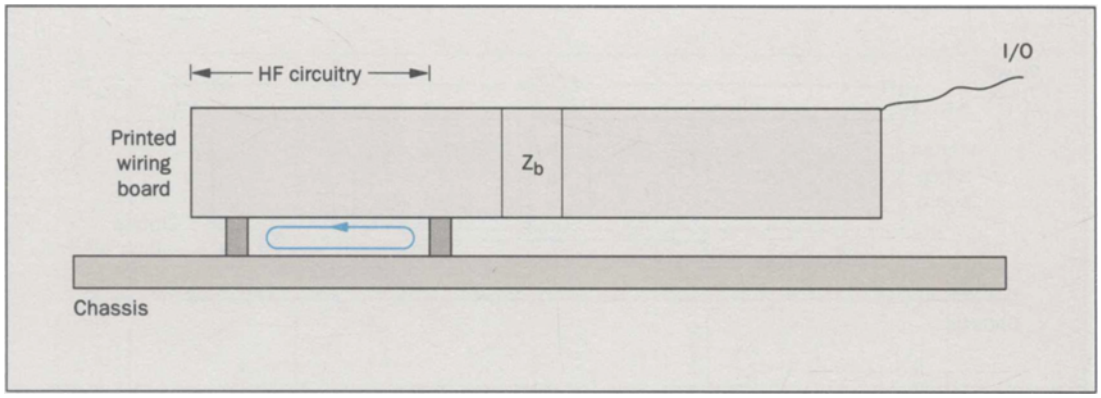

Figure 6. A desired configuration for a board where the RF circuitry can be contained in a small area. The stitches surrounding the RF circuitry cause local eddy currents to flow in the board, stitches, and chassis under the RF circuitry. The rest of the board is at ground potential, and an I/O lead exiting the right side of the board will not radiate significantly.

card-cage frame, causes increased RF currents to flow in the card cage and increases the voltage drop E3. E3 can be lowered by including a chassis plane between the backplane's ground and power planes. The chassis plane should be connected to the chassis frame every couple of inches. Figure 7b shows an end view of the backplane. Signal layers and other ground layers would be added to the outside the structure shown. A good chassis plane can lower E3 to the 10 to 20 millivolt range.

To reduce E3 significantly, typically 20,000 pF of capacitance is needed between the chassis plane and both the power and ground planes, for a total of 40,000 pF. Using a 10 mil dielectric of FR4 material, this translates to a capacitance of 90 to 100 pF/square inch. Therefore, about 200 square inches of area is needed plus area for vias, holes, and pins.

Etching of ground and power planes for better adhesion increases the planar impedance, in units of ohms per square, by about 10 dB over smooth ground planes. This can lead to increased common-mode noise voltages in both PWB's or backplanes.

Formal System Design for Planning and Metrics

Formal quality systems must be in place for both EMC planning and metric aspects of product realization. In this context, *metric* refers to a measurement system used to determine compliance with predetermined requirements or guidelines. Effective EMC planning before development will ensure that the correct electromechanical and electromagnetic technologies are chosen to achieve maximum compliance with all applicable mandatory product requirements. Organizations such as the AT&T Global Product Compliance Lab, the Electrostatic Discharge Studies Group of the Manufacturing Systems Engineering department, and the Quality Assurance Center can be consulted to help set up formal processes for product standards compliance planning, design implementation, process metrics to ensure compliance and conformity assessment testing.

The importance of quality measurement and verification processes cannot be overemphasized. The only assurance that designs are working toward compliance is to establish a series of tracking metrics that are specific and customized to account for all aspects of the product specification, design, and test processes related to EMC. Product realization quality systems of this level clearly define process ownership, responsibility, flow, and details specific to process implementation. AT&T is adopting the quality initiatives set forth by the International Standards Organization and will be required to develop and thoroughly document these types of quality processes to meet such mandatory standards as those of the EC.

Conclusions

International business markets are expanding, and present a significant challenge for multinational corporations such as AT&T. Those who will thrive will offer products and services that consistently comply with international mandatory standards and exhibit a

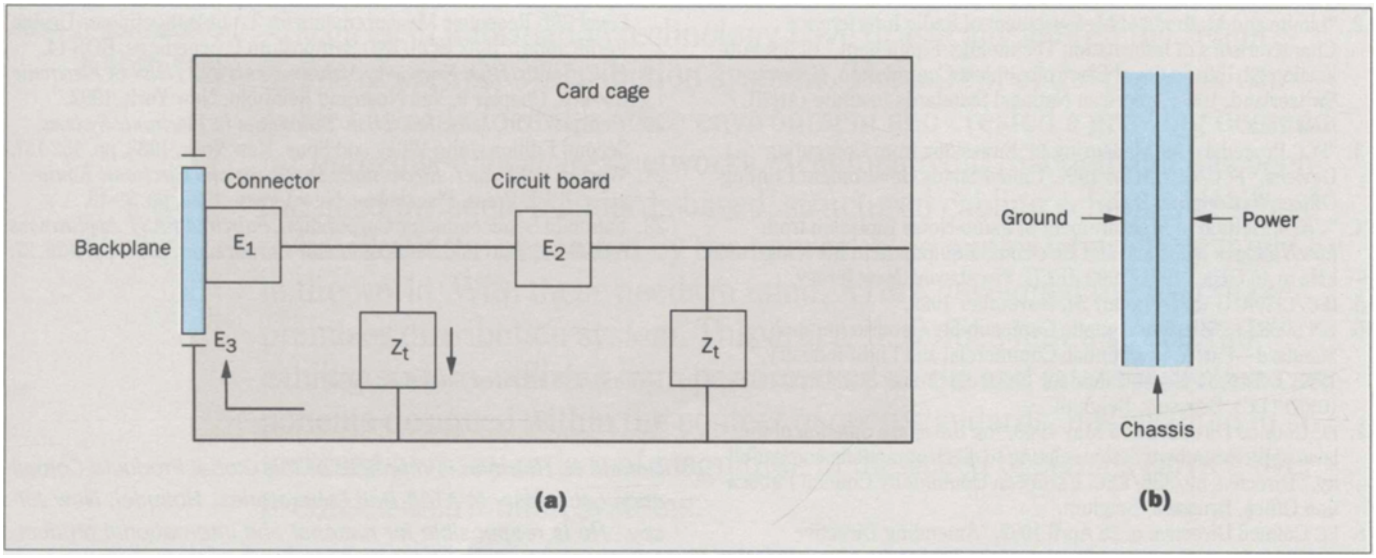

Figure 7. A circuit board with added shielded cable at its right side (7a) with the shield attached to the card-cage frame. This causes increased RF currents to flow in the card cage, and increases the voltage drop E3. E3 can be lowered by including a chassis plane between the backplane's ground and power planes. The chassis plane should be connected to the chassis frame every couple of inches. (7b) shows an end view of the backplane.

comfortable margin with respect to minimum compliance levels. Many will be judged not only on their record of compliance to a demanding set of requirements, but also on the merits of their quality systems addressing all aspects of EMC as well. Hence, designing for international standards compliance:

- Addresses AT&T's mission to achieve globalization in product and service markets.
- Enhances functional performance of both the product realization team and the overall quality of the product itself.
- Enables AT&T to achieve new dimensions in customer satisfaction and quality.
- Results in a significant reduction in development time and cost when taking into account the delay and effort associated with redesigning products with inadequate EMC hardware and electronics design.
- Eliminates a less effective course of action is to meet EMC requirements on a country-by-country basis by redesigning products after the initial design is complete.
- Requires an integrated approach to the product realization process by using quality systems and metrics that are recognized internationally. This is especially true in meeting international RF immunity standards more stringent than those in the United States.

In terms of compliance to mandatory standards, manufacturers having difficulty bringing products to the international marketplace will be branded as unreliable providers of products and services. These firms will quickly find themselves alienated from both present and future market opportunities. They will effectively push themselves out of the market. In addition, manufacturers that delay in adopting the international standards and the quality systems required for successful market penetration will fall hopelessly behind the leaders in terms of market share.

Acknowledgments

We thank Dheena Moongilan of the Global Product Compliance Laboratory of AT&T Bell Laboratories in Holmdel, New Jersey, and Michael King, a noted EMC authority who has presented a series of lectures to the AT&T Bell Laboratories Research & Development community.

References

1. Donald Heirman, et. al., "Design for Multinational EMC Compliance," *AT&T Technical Journal*, Vol. 69, No. 3, May/June 1990, pp. 28-45.

2. "Limits and Methods of Measurement of Radio Interference Characteristics of Information Technology Equipment," CISPR Publication 22, International Electrotechnical Commission, Geneva, Switzerland, 1985; American National Standards Institute (ANSI), New York.
3. "FCC Procedure for Measuring RF Emissions from Computing Devices," FCC/OET MP-4 1987, United States Government Printing Office, Washington, D.C.
4. "C63.4 Method of Measurement of Radio-Noise Emission from Low-Voltages Electrical and Electronic Equipment in the Range of 9 kHz to 40 GHz," 1991/1992, IEEE, Piscataway, New Jersey.
5. IEC/CISPR/G (Secretariat) 34, November 1992.
6. EN 50082-1, "Electromagnetic Compatibility Generic Immunity Standard—Part 1: Residential, Commercial and Light Industry," 1991, European Organization for Electrotechnical Standardization (CENELEC), Brussels, Belgium.
7. EC Council Directive of 3 May 1989, "on the approximation of the laws of the Members States relating to electromagnetic compatibility," Directive 89/336/EEC, European Community Council Publication Office, Brussels, Belgium.
8. EC Council Directive of 28 April 1992, "Amending Directive 89/336/EEC on the approximation of the Law of the Member States relating to electromagnetic compatibility," Directive 92/31/EEC, British Standards Institute (BSI), United Kingdom.
9. EC Council Directive of 29 April 1991, "on the approximation of the laws of the Member States concerning telecommunications terminal equipment, including the mutual recognition of their conformity," Directive 91/263/EEC, British Standards Institute (BSI), United Kingdom.
10. EC Council Decision of 13 December 1990, "concerning the modules for the various phases and the conformity assessment procedures which are intended to be used in the technical harmonization directives," Decision 90/683/EEC, British Standards Institute (BSI), United Kingdom.
11. EC Council Directive of 19 February 1973, "on the harmonization of the laws of Member States relating to electrical equipment designed for use within certain voltage limits," Directive 73/23/EEC, British Standards Institute (BSI), United Kingdom.
12. ISO Standard 9002, "Quality Systems—Model for Quality Assurance in Production and Installation" (equivalent to European Norm EN 29001), 1987.
13. ISO Standard 9001, "Quality Systems—Model for Quality Assurance in Design/Development, Production, Installation, and Servicing" (equivalent to European Norm EN 29001), 1987.
14. IEC-801-4, "Electromagnetic Compatibility for Industrial Process Measurement and Control Equipment: Electrical Fast Transient/Burst Requirements," International Electrotechnical Commission, 1988 (available from the American National Standards Institute, 1430 Broadway, New York, N.Y. 10018, 212-642-4987).
15. Henry W. Ott, *Noise Reduction Techniques in Electronic Systems*, Second Edition, John Wiley and Sons, 1988, Chapter 11.
16. Warren Boxleitner, *Electrostatic Discharge and Electronic Equipment*, IEEE Press, 1989, pp. 21-25.
17. Henry W. Ott, *Noise Reduction Techniques in Electronic Systems*, Second Edition, John Wiley and Sons, 1988, pp. 166-169.
18. D. C. Smith, "Techniques and Methodologies for Making System Level ESD Response Measurements for Troubleshooting or Design Verification," 1992 EOS/ESD Symposium Proceedings, EOS-14.
19. D. C. Smith, *High Frequency Measurements and Noise in Electronic Circuits*, Chapter 9, Van Nostrand Reinhold, New York, 1992.
20. Henry W. Ott, *Noise Reduction Techniques in Electronic Systems*, Second Edition, John Wiley and Sons, New York, 1988, pp. 152-157.
21. Warren Boxleitner, *Electrostatic Discharge and Electronic Equipment*, IEEE Press, Piscataway, New Jersey, 1989, pp. 39-48.
22. Fairchild Semiconductor Corporation, *Fairchild FAST Applications Handbook*, Fairchild Semiconductor Corporation, 1987, pp. 9-26, 27.

(Manuscript received August 7, 1992)

Donald N. Heirman *is manager of the Global Products Compliance Laboratory at AT&T Bell Laboratories, Holmdel, New Jersey. He is responsible for national and international product conformity assessment to mandatory standards and regulations in the areas of EMC, product safety, and telephone network interconnect. He joined AT&T in 1963 with a B.S.E.E. and M.S.E.E. from Purdue University, West Lafayette, Indiana.*

Steven M. Crosby *is a senior technical associate in the Engineering Information, Standards and Commercial Art department of AT&T Bell Laboratories, Middletown, New Jersey. He is currently involved in process of co-developing a Best Current Practice database on EMC product realization techniques and mandatory product standards, and is the factory interface/consultant for printed wiring boards designed for the AT&T Richmond Works. He joined AT&T in 1985 with an A.A. in Business Administration from Bergen Community College, Paramus, New Jersey, and is completing a B.S. in electrical engineering from Rutgers University, New Brunswick, New Jersey.*

Douglas C. Smith *is a distinguished member of technical staff in the Manufacturing Systems Engineering Department of AT&T Bell Laboratories, Middletown, New Jersey. He is responsible for studying high-frequency measurements and noise in electronic circuits and systems. He joined AT&T in 1969 with a B.E.E.E. from Vanderbilt University, Nashville, Tennessee; and an M.S.E.E. from the California Institute of Technology, Pasadena.*