Achieving Customer Satisfaction Through Robust Design

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A winning product has to consistently outperform its rivals by providing value in today's highly competitive markets. At the heart of consistent value is robust design — the process of ensuring that a product will perform well despite variations in raw materials, components, manufacturing, and operating conditions. It consists of steps for identifying key parameters that affect the customer, analyzing to predict and improve robustness, and measuring to confirm performance. As it exists in AT&T's Transmission Systems Business Unit (TSBU) for hardware development, robust design is a real, effective process. It should be used to ensure design robustness for all designs, especially those intended for multi-use platforms.

Introduction

The robust design process is expected to improve the quality of product performance, reduce the number of development cycles and life-cycle costs, and increase revenue growth in AT&T's TSBU. Design robustness is one of many factors that can improve product performance and factory yield, and lower failure rates and field returns. Other factors include manufacturing process quality, component quality, and training and maintenance policies.

Our leap of faith is that these benefits will result, in varying degrees, but that the principal benefit of robust design will be the delight our customers take in the consistency and value of our products. The robust design process not only leads to a design environment that is conducive to making products that satisfy and delight customers, but also provides a quantitative measure of design quality from the customer's perspective, as we will discuss later.

There have been over a dozen applications of robust design as a result of the TSBU's Six-Sigma Robust Design (SSRD) project. As more multi-use and reusable designs are created, applications of robust design will increase. Robust design has been applied at the component level, the circuit-board level, and the equipment level. We continue to learn how to evaluate, improve, and measure mechanical, digital-circuit, and analog-circuit design parameters.

Data obtained from the TSBU 1-in-10,000 reliability project indicate that design has a strong influence on the rate of product return. Robust products that perform near perfection "straight out of the box" are more reliable and have a longer life than those that are marginal. Robust design is also associated with other quality activities.

It is important for the robust design process to be built on a concurrent engineering foundation, which combines process concurrency and cross-functional teams (CFTs).[1] CFTs are invaluable, in part, because the manufacturing and testing functions are in-house customers of the design. Manufacturing tests need to be developed along with product design, so that data can be collected during the early stages of product development, as well as during production, to validate robust design analyses. If a design is robust enough to withstand manufacturing and testing vagaries, it will also perform well in the end-user environment.

Robust design is tied to the APEX[2] (Achieving Process Excellence) interval reduction project in the TSBU. (APEX is a dynamic process management structure used to identify and deploy leading-edge practices.) Ultimately, robust design must be seamlessly integrated into the whole

development process. Product consistency, along with market window, cost, schedule, features, and reliability, must drive activities in each phase of development. The types of integration needed to perform robust design are in the areas of computer-aided engineering (CAE), test methodology, and component sourcing.

In 1992, SSRD was specifically audited by the examiners for the Malcolm Baldrige National Quality Award (MBNQA). Because robust design is considered a leading-edge quality initiative, its activities generate considerable interest and focus in the electronics industry. Like AT&T's TSBU, which won the MBNQA in 1992, other MBNQA-winning companies, such as Motorola,[3] Texas Instruments, and IBM, have robust design programs.

SSRD in the TSBU would not have been possible without the contributions from Motorola's Six-Sigma Quality program, which led to their winning the MBNQA in 1988. The SSRD is patterned after Motorola's program, and this paper primarily deals with our progress in making Six-Sigma Quality (SSQ) real in the TSBU.

The TSBU Six-Sigma Robust Design Project

SSRD has defined its brand of robust design as follows:

"Robust Design is one of the Quality Planning Matrix projects deployed by the TSBU to achieve high levels of customer satisfaction with the performance of our hardware projects. It is the disciplined practice of variation reduction and performance centering relative to key customer requirements.

Robust Design requires that the variation in performance for those parameters that are key to customer satisfaction be determined during design and manufacture. Capability indices, such as C_p and C_{pk}, are metrics which compare this variation to the customer's limits of acceptable performance. When the capability indices equal or exceed 2 and 1.5, respectively, the product is of Six-Sigma Quality and the design is considered to be robust."

Robust design has two objectives: first, to minimize the product variance, so that product variation is small with respect to customers' tolerance limits; and second, to eliminate the product bias, so that the nominal product is equal to the customers' ideal product. Prediction and improvement are performed during development, and then measurement and any necessary remedial action are taken during manufacturing, as shown in Figure 1.

SSRD is principally concerned with keeping the location and spread of the product parameters within the customers' tolerance limits, rather than eliminating all defects that have parameters outside their limits. SSRD analyses do not require precise knowledge of distributions. The populations shown in Figure 1 are for illustrative purposes only, since robust design metrics can handle many distribution types.

To predict and improve the design, necessary ingredients include:
- Knowing the extent of variation in the components, processes, and user environment,
- Being able to experiment with either hardware or software models,
- Having the appropriate metrics to evaluate the quality of the design, and
- Using effective and efficient optimization strategies.

To measure and act on products during manufacture, we need the ability to test the parameters of components
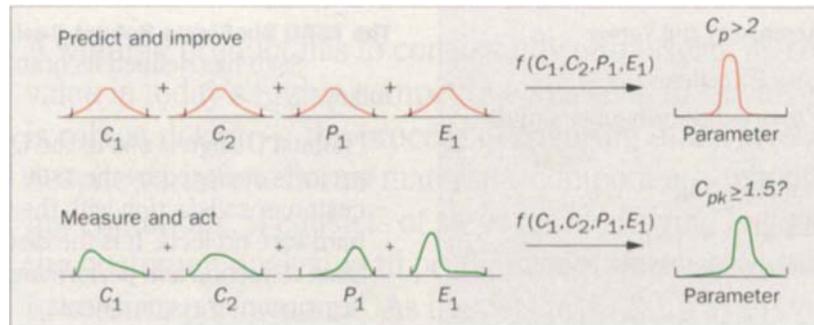
Figure 1. Robust design is used on any parameter that is key to customer satisfaction. First, the distributions of its major noise factors (component, process, and environment) are estimated. Then the parameter's input/output relationship (f) is evaluated to predict response variation. The design is analyzed and changed until its quality level is SSQ. Next, actual parameter variation is measured. If SSQ is not confirmed, then remedial activities begin.

and products while they are subjected to stressful environments, to collect and store statistics, and to retrieve parametric data regularly for analysis and action.

The SSRD Process

SSRD is achieved by following a process of planned robust design activities. The robust design process takes many forms, but all follow several basic steps. Figure 2 shows the SSRD process, based on the seven steps of the Quality Improvement Story (QIS),[4] which is widely used in the TSBU.

In step 1, the CFT begins the robust design process by discovering what will satisfy the customer. Step 1 and step 2, described in the next paragraph, can be accomplished using an available quality function deployment (QFD) tool, which helps to ensure that customer needs are included throughout the requirements, design, and manufacturing stages of product development.

In step 2, the CFT begins to understand how to satisfy the customer by translating customer requirements into measurable engineering characteristics and by assigning limits based on quantifiable customer tolerances. The CFT then identifies the major causes of product variation and their patterns of behavior at this time. Last, the CFT pinpoints one or several design configurations that will likely meet the features, cost, robustness, reliability, safety, etc. requirements of the design.

In step 3, the CFT assesses the effects of variation on the design configurations. The statistics of critical parameters are evaluated in terms of C_p and C_{pk} (see Panel 2).[3] If a design is not up to SSQ standards, it is incrementally improved in step 4 until SSQ is reached. Any combination of variation analysis and design optimization packages may be used iteratively in steps 3 and 4.

One approach that can be used in steps 3 and 4 is called the Taguchi Method (see Panel 3).[7,8] It offers analysis and optimization using a unique data transformation, called signal-to-noise ratio (S/N), and matrixed orthogonal array experiments. It is not, however, part of any major CAE tool, so other CAE-accessible approaches are often used. Monte Carlo, worst-case, random search, sequential quadratic programming,[11] and response surface methodology[12] are examples of analysis and optimization approaches found in CAE tools.

In step 5, the CFT confirms that the predictions and improvements made in steps 3 and 4 correlate to actual performance, by obtaining parametric measurements from the factory and, possibly, the field. The statistics are summarized in terms of C_{pk} and compared with the design intent. Measured C_{pk} is a true indicator of design robustness; our leap of faith is that it leads to customer satisfaction.

In step 6, the CFT uses standard test procedures to ensure that the product continues to meet the robustness goal of SSQ. The CFT also ensures that its efforts can be reused in similar products, by documenting its experience and including reusable findings in design guidelines and checklists.

In step 7, project teams forecast new products that will be designed, and begin to plan for robust design in those products. Through its experiences, SSRD has found that projects not only need to plan ahead for the robust design process, using project management to staff
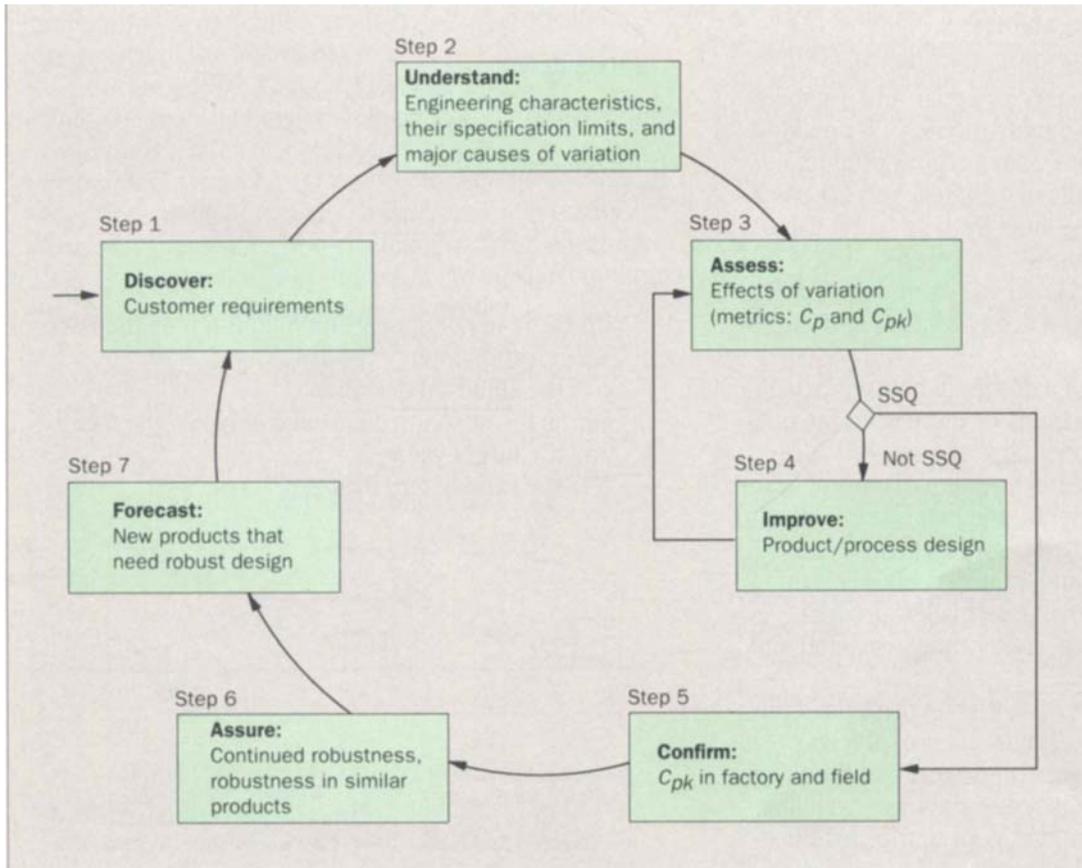
Figure 2. The robust design process had QIS-like steps: (1) discover (reasons for improvement), (2) understand (current situation), (3) assess (analysis), (4) improve (counter-measures), (5) confirm (results), (6) assure (standardization), and (7) forecast (future plans).

the appropriate CFTs, but also need to support and schedule their robust design activities.

Historical Factors

The development and deployment of the SSRD process have been influenced by historical factors from a number of sources. Among these are:

- Motorola's contribution of SSQ metrics (see Panel 2);[3]
- Florida Power and Light's contribution of the Quality Improvement Story (see Figure 2);[4]
- Taguchi's contribution of variation reduction using designed experiments (see Panel 3);[7]
- Policy deployment approach using the TSBU quality planning matrix (QPM), which disseminates executive policies through the entire business unit; and
- Approaches for ensuring product quality, such as worst-case study and defects analysis.

The latter two factors have a strong effect on the direction and success of robust design deployment, its goal

being to transform the design process so that robust design becomes an everyday part of business.

First, there is no substitute for direct involvement by executive leaders. QPM has worked extremely well for the TSBU as a deployment vehicle for quality projects. From the president of TSBU down, there is empowerment and support for TSBU quality projects such as SSRD. QPM projects address issues such as customer satisfaction, customer feedback, manufacturing processes, financials, business processes, product returns, software quality, front-end processes, product realization, provisioning, customer-support services, employee involvement, leadership, and profitable growth.

Second, changes to deeply ingrained design traditions have to be treated with sensitivity to encourage grass roots support. From the start of the project, great effort has been made to involve the users of the SSRD process in its development. Engineers and managers from all TSBU hardware projects are encouraged to participate

Panel 2. Six-Sigma Quality Metrics

Motorola, which won the MBNQA in 1988, has pioneered Six-Sigma Quality as a goal, and capability indices (C_p and C_{pk}) as quality metrics.[3] By making two practical assumptions, that a typical product parameter: (1) is normally distributed, and (2) has a mean that is shifted 1.5σ units from its target value, Motorola showed that an SSQ design has a defect rate of 3.4 parts per million. Under the same assumptions, a three-sigma design has a defect rate of 66,810 parts per million.

The robustness of a design to natural variation can be increased 20,000 times by increasing the quality of the design from three-sigma to six-sigma. In other words, after accidents from out-of-control usage, documentation, components, and manufacturing processes are eliminated, design robustness is a major cause of defects, and, hence, customer complaints. As defect rates become smaller, product defects must be designed, rather than inspected, out of products.

Rather than focus primarily on the tails of the product distribution (i.e., the number of defects), SSRD focuses on the performance of the main product distribution. This is where robust design is most valuable. Is the product population that goes to the customer tightly centered about the target value? To answer that question, SSRD uses the quality metrics of C_p and C_{pk}, as recommended by Motorola. Statisticians have examined many forms of these indices, in depth, as well as their properties, advantages, and appropriate usage.[5,6] The simplest forms are defined for parameters with a normal distribution and bilateral specification limits:

$$C_p = \frac{\Delta}{3\sigma}$$
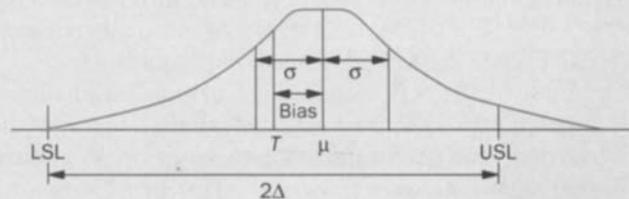
$$C_{pk} = \frac{\Delta - |bias|}{3\sigma} = C_p (1 - K)$$

where:
  2Δ is the upper specification limit minus the lower specification limit
  σ is the standard deviation
  bias is the absolute difference between the mean and the target value
  K is the ratio of *bias* over Δ.

T – Target value	2Δ – Specification width
μ – Population mean	LSL – Lower specification limit
σ – Standard deviation	USL – Upper specification limit

Motorola[3] determined that natural variation can cause the mean to deviate, on average, about 1.5σ units from its target, i.e., *bias* equals 1.5σ. For a product to be SSQ, i.e., Δ equals 6σ, it has to have C_p greater than or equal to 2.0, and C_{pk} greater than or equal to 1.5.

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in the three robust design steering committees:
- The Functional Task Team (FTT),
- The Robust Digital Design Team (RDDT), and
- The Robust Physical Design Team (RPDT),

which have core memberships representing over a dozen development organizations. These teams will be discussed later.

SSRD Project Beginnings

The SSRD project began without much fanfare around mid-1990, as a direct result of the leadership provided by Pete Fenner, president of TSBU at that time. He and his executive management team started the QPM and the TSBU quality program. One of 25 individual projects in the QPM, robust design had, as its fundamental objective, "enhancing our quality."

The influence from Motorola's SSQ program undoubtedly was a key factor. Before the advent of the business-unit-wide effort to support robust design, there were only isolated instances of robust design studies in the TSBU. These used design of experiments, e.g., on a circuit-board connector mating problem from the Satellite Communications Laboratory. A rapid change was needed, from individual robust design experiments to

Panel 3. How a Taguchi Experiment Works

During the 1980s, Taguchi experiments heavily influenced the development of robust design in AT&T, especially in integrated circuit process development and manufacturing process improvements.[9,10] Tens of experiments were run each year, many of which were leading-edge studies that explored new areas of applications.[8,9] In particular, product design applications increased in the late 1980s.

Since 1980, Taguchi practitioners, including Taguchi, have had major changes in their thinking. For example, the idea of simulating the noise regime using orthogonal arrays has given way to the more practical idea of compounding many noise factors. In essence, a Taguchi optimization experiment is a relatively quick way of systematically evaluating many design configurations under several worst-case conditions.

Here is a simple illustration of how a Taguchi experiment works. The following ac circuit, with a resistor and inductor in series, needs to have its output current optimized. (Other goals and constraints for this circuit are not considered here.) Its engineering equation can be derived from Ohm's Law:

$$I = \frac{E}{\sqrt{R^2 + (2\pi f L)^2}}$$
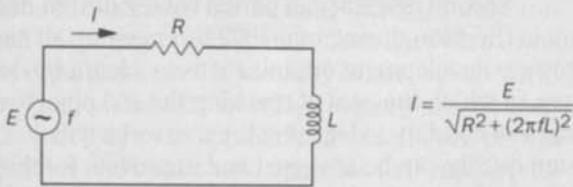
The customer requirements call for a target value of 10 amperes and a tolerance of 2.5 amperes. The power source has a voltage of 100 VAC with a tolerance of 10 percent, and a tightly toleranced frequency of either 50 or 60 hertz. The resistor and inductor are initially selected as 10-percent tolerance parts with nominal values of 5 Ohms (Ω) and 0.02 Henry (H), respectively. The nominal values of the resistor and inductor can be adjusted to make the circuit more robust. Temperature and degradation effects have been included in the component tolerances.

Since the circuit equation is explicitly known, we can actually optimize this circuit without a Taguchi experiment. By making some practical assumptions, that the component parameters are statistically independent and have their limits at three standard deviations from their nominal values, we can solve the following variance equation:

$$\sigma_I^2 = \left[\frac{\partial I}{\partial E}\right]_C^2 \sigma_E^2 + \left[\frac{\partial I}{\partial R}\right]_C^2 \sigma_R^2 + \left[\frac{\partial I}{\partial f}\right]_C^2 \sigma_f^2 + \left[\frac{\partial I}{\partial L}\right]_C^2 \sigma_L^2$$

where ∂ is the partial derivative and C is the evaluation at nominal values.

To minimize variance and maintain a typical current of 10 amperes, the optimal values of R and L turn out to be 8Ω and 0.017H, respectively. Its corresponding capability index, C_p, is 1.9. At this point, adjacent standard R and L values may be selected. Additional steps include considering alternative design configurations that may be more robust, or doing economic tradeoffs by reducing one or several component tolerances, while possibly increasing the tolerance of another component.

The partial derivatives in the variance equation are called sensitivity coefficients. Design robustness is not costly when these coefficients are small. Taguchi experiments work primarily because they can reduce most of these coefficients without having to know or solve explicit engineering equations. This type of situation occurs in many design problems, so a set of Taguchi experiments can be an inexpensive way to minimize variance and still achieve the target value.

Assuming the engineering equation for this ac circuit is unknown, this is how a Taguchi experiment would be done: *A priori* engineering knowledge provides a starting point for the experiment. An orthogonal array that yields nine combinations of nominal resistor and inductor values is selected (it is actually a full factorial, since there are only two parameters). Each combination is then subjected to a minimum of two worst-case noise conditions (more noise conditions, e.g., using an orthogonal array, are necessary when more accurate statistical analysis is desired).

The two data points for each combination are transformed into estimates of a mean (the signal) and an error variance (the noise). The most important summary statistic is the S/N.[7,8] The orthogonality property allows analysis of means (ANOM) to be done on the nine S/N values, so that the main effect of each parameter on S/N can be independently assessed. The parameters that have large effects on S/N will have their values adjusted so that S/N is maximized. Then the parameters that have small effects on S/N and large effects on the signal will have their values adjusted so that the overall mean is on target.

In some cases, as with this circuit, it may not be clear which parameter should be used to adjust the mean rather than S/N, because all design parameters affect S/N almost equally. Another issue to watch out for is the possibility that two or more parameters affect S/N dependently, that is, the value of one parameter controls another parameter's main effect on S/N.
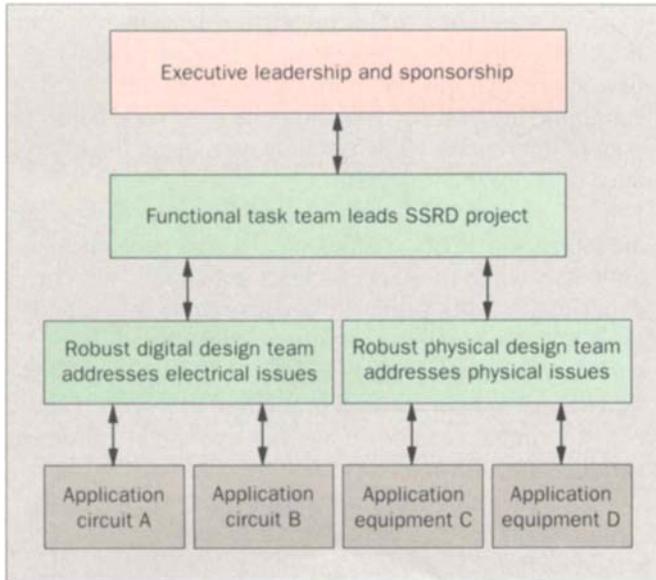
Figure 3. The SSRD project started as a single FTT made up of hardware department heads who volunteered to apply robust design to their products. Soon, focus teams were needed to address ease-of-use issues, such as tools, data, and metrics for circuit and physical designs. A critical success factor for the teams has been the coordination and guidance from QUEST robust design specialists. Engineers conducting individual applications can go to these teams for training, coaching, and support.

integration of robust design into the design process.

In July 1990, after hardware department heads were asked to develop and deploy a process for design of robust products, they met to form an FTT that conformed with the policy deployment management structure, now known as the TSBU robust design FTT. At this first meeting, QUEST robust design specialists described metrics definitions, statistical techniques, process changes, and team facilitation, all of which would be necessary to get the SSRD project started and deployed.

SSRD has the detailed objective of improving hardware quality and reliability by improving key design processes. The goal set by the FTT was, and is, to achieve SSQ on new hardware designs by the end of 1996. To reach this goal, the FTT set two early milestones, pivotal to the success of SSRD, both of which were achieved.

First, SSRD met its goal of performing and documenting a half-dozen pilot robust design applications by 1992. The pilots demonstrated the usefulness of robust

design, but at the same time showed the current difficulties of performing it full-scale. Simple time-saving methods and tools are needed to make robust design an everyday design practice, rather than a specialized effort. Robust design currently does not come "out of the box" ready to use.

This theme was common in all six pilot applications, two being mechanical design of circuit-board insertion into equipment shelves, two being the design of microelectronic components, and two being the design of electronic circuits — one analog and one digital. Taguchi optimization methods were not used in any of these pilots. Instead, these pilots led directly to the formation of two robust design focus teams, RDDT and the RPDT, both of which act as the voices for their respective TSBU robust design user communities.

Second, SSRD began partial robust design deployment in the TSBU during mid-1992 by engaging all its hardware development organizations in a learn-by-doing phase, in which the goal of reaching the SSQ objective became secondary to learning the means by which design quality can be assessed and improved. Robust design deployment was assigned during an SSRD kick-off meeting, called and chaired by SSRD's coordinating executive, at which all department heads with hardware development responsibility were represented.

During this time of learning, the FTT leadership directed a QIS team of key SSRD people to analyze the pilot experiences. The QIS team identified user issues that needed to be resolved between 1992 and 1996 to meet the goal of fully deploying the robust design process. To ensure successful and complete deployment, the FTT set the following countermeasures:

- Top-down management commitment, involvement, accountability, and follow-through;
- Proof of value ("worth the effort") in economic terms;
- Ease of use in methodology, CAE tools, factory data collection, and component data availability; and
- Integration into the development process using the APEX project.[2]

To accelerate effective and practical robust design deployment, SSRD activities are now geared to address these measures fully.

SSRD Project Progress

Today, Greg Hughes, president of TSBU, provides leadership for the entire TSBU quality program that Pete Fenner initiated. SSRD continues to be managed as

though it were a development project, with tracking of milestones, goals, resources, and staffing. Figure 3 shows the SSRD project structure. Many engineers and managers who were involved in the pilots are now the pro-active core of the SSRD project team structure. In response to the finding by the QIS team that factory and component data are crucial to the process of making designs robust, manufacturing managers have joined the robust design teams.

The FTT, which in 1993 contained three TSBU hardware department heads, three manufacturing managers, and two QUEST robust design specialists, provides overall leadership for the project. It works within the policy deployment process, which starts at the top levels of the TSBU. The FTT negotiates QPM objectives, and, each year, establishes detailed project milestones to ensure that those objectives will be met. One such milestone is to get 100-percent participation from hardware development organizations. This activity is now being carried through the hardware development organizations using a policy deployment approach, in which each person negotiates and commits to activities that support the commitments made by their leaders. The FTT helps by bringing attention to the SSRD project and by coaching their colleagues.

Development projects that apply robust design techniques can get support through the RDDT for circuit robust design, and through the RPDT for mechanical robust design (see Figure 3). These teams have representatives from across many development projects, and membership continues to include development and manufacturing engineers from new applications. The primary responsibilities of these two teams are to work with development projects to make robust design easier to use across product lines, increase manufacturing involvement, and help the TSBU build the robust design infrastructure.

The countermeasure to improve ease of use is being worked on, as evidenced by recent RDDT and RPDT activities. For example, the RDDT has developed a robust design tool for digital timing design that is integrated with a CAE circuit-simulation environment (see Panel 4). Similarly, the RPDT has evaluated commercially available simulation tools for mechanical design that can be used "as is" or adapted for SSRD.

Another example of a countermeasure to make robust design easier to use is the work to address availability of component parameter data, such as typical (average) values, minimum and maximum limits, distributions, and application-specific characteristic curves. Early supplier involvement is essential. Robust design evaluation and optimization can be drastically affected if key noise factors are grossly misrepresented. Therefore, subteams of both teams are seeking practical ways to obtain or infer statistical data from suppliers and the factory to facilitate robust design analyses. Robust design requires that the CFT has, or can collect, information on the behavior of noise factors, and then is able to confirm in the factory whether the design requirements are being met.

As the learning phase tails off and more integrated robust design applications become the norm, the TSBU QPM will revise the SSRD project goals to focus on designing the SSQ product, instead of participating in and learning about the SSRD project. This shift to customer-focused goals will be gradual. For example, the RDDT and RPDT are beginning to coach new SSRD applications that are evaluating and improving the capability indices on key parameters, as well as making robust design easier to use.

SSRD Project Future

SSRD has changed over the past two years, and will evolve more as 1996 draws nearer. The SSRD project has already overcome many problems. A common metric, called the *capability index*, was adopted from Motorola for evaluating design quality. A digital-circuit timing design tool has been developed. Most hardware development departments have participated in SSRD. Tens of TSBU robust design applications have been documented. Concurrent engineering teams are more interested than ever in robust design. The TSBU Wired Equipment Team, which is developing common equipment for use across the TSBU, plans to use robust design on all multi-use platforms.

The SSRD project has a number of remaining challenges to meet. One is the difficulty of translating supplier specifications into a robust design context. The belief that a design is robust hinges on how well the CFT understands the major sources of variation and their distribution limits. A component parameter defined by a minimum value and a maximum value can have very different distributions, depending on its suppliers and their processes. In addition, most limiting values are specified to include effects of thermal variation, lifetime degradation, and engineering safety factors. Therefore, early involvement of critical component suppliers in the development process — another basic element of

Panel 4. A Tool for Robust Digital Timing Design

Robust design of digital timing margin is usually straightforward, because its response is linearly related to its components' timing parameters. However, complexity is added when factors such as temperature, degradation over time, and correlation of gates in the same device have to be independently addressed in the analyses.

Other issues also encumber digital robust design analyses, such as the large number of devices and nets on most boards, the difficulty of translating device specifications into robust design terms, and the need to iterate until SSQ is achieved.

Following TSBU robust design needs and QUEST specifications, the System Simulation Tools Group of the Computer-Aided Design and Test Laboratory in AT&T Microelectronics has developed a computer-aided design feature called K-Sigma, which is flexible enough to handle these problems. It is available in the ATTSIM simulation product scheduled for production release in mid-1994.

Prior to this release, ATTSIM used minimum and maximum component delays to accumulate ambiguity regions, which are bounded by the earliest and latest times that the signal can change value. Though common ambiguities that arise as paths reconverge are taken into account, results can often be pessimistic and, sometimes, optimistic, depending on the number of components that contribute variation to the paths and the correlation between components.

With the K-Sigma feature, ATTSIM accumulates the mean and variance of signal transition times at each component. Using the distribution parameters, ATTSIM computes the sigma quality metric ($Q = 3C_p$) for each timing constraint, and audits it against a specified value, 6, by default, which corresponds to SSQ.

The maximum and minimum component delay values are assumed to be $\pm 3\sigma$ from the mean value, unless the user redefines the assumption. Given these maximum and minimum delay values, ATTSIM calculates the

$$mean = \frac{(min + max)}{2,} \text{ and}$$

$$\sigma = \frac{(max - min)}{6}$$

for the component delay distribution.

During simulation, ATTSIM adds the mean component delay to the mean of the input signal distribution to obtain the mean of the output signal distribution. The sigma for the output distribution is calculated as the square root of the sum of the squares of the input sigma and the sigma of the component distribution. The output sigma is adjusted if there is correlation between the component and any components in the input signal path. For example, when two gates are completely positive-correlated, twice the product of the gates' sigmas are subtracted from the output sigma. Common ambiguity is treated as a special case of correlation in which the same component contributes twice to the output sigma. Similar procedures are followed when timing constraints between signals are audited.

The Q value is computed and checked whenever a timing constraint check is performed, and when checking for spikes and glitches on combinational elements. If Q is less than k, as specified by the $-k$ option, then the violation is shown on Output Display And Analysis (ODAN) windows and a report is written into a K-Sigma audit file. The reports, used for debugging, give the amount of sigma that each component in the path has added to the signal transition time.

All uniquely computed Q values are then used to generate a K-Sigma histogram report for the overall design. A design with most Q values between 6 and 10 can be expected to be consistent and cost-effective.

concurrent engineering — is essential for robust design to work well.

Another challenge is the availability and use of testing equipment and staffing in the factory to sample and analyze the parameters of data. New testing infra-structures need to be developed, including methodologies, possible equipment changes, and modifications of staff assignments. Along with this, an organized system needs to be developed for storing and retrieving parametric data during product development. We need to

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move away from the established process of "testing-in" quality, and toward a process of "designing-in" quality.

These challenges are currently being dealt with on a case-by-case basis. In the future, applications will be richer, in depth as well as breadth. Because of the SSRD support structure, we will find common elements in what may seem to be different applications. This knowledge will help us to resolve these challenges more easily, and will satisfy the increasing need for robust designs as multi-use and reusable platforms become the development norm. By 1996, we expect robust design to be integrated into the TSBU development process. This can only be accomplished by using global design procedures and rules that cut across product lines.

Conclusion

To achieve consistency and value in AT&T's products, the TSBU is committed to real, effective, and practical applications of robust design during product development. Our SSRD project is developing the framework needed to make products that meet the SSQ standards. Pieces of the framework include tools, methods, process steps, and applications benchmarks. We have found that the success factors of such an undertaking are a high-quality blending of management, teams, data, pilot, and deployment activities.

Although our story is not complete, we hope that this paper will encourage greater use of robust design within the TSBU, across other AT&T business units, and in other companies. Much more can be done to move from isolated applications to a structured, reusable process. With executive commitment to an integrated robust design development process, we can overcome cultural resistance, the pressures of tight schedules, and short-term thinking about product quality.

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