Testing Goes Critical Path

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Within the past few years, testing technology has become a critical, limiting factor in manufacturing leading-edge products at competitive cost and quality. In this paper, we highlight key drivers for this phenomenon, and outline some of the emerging approaches to testing. These approaches are more fully described in the articles in this issue of the *AT&T Technical Journal.*

Introduction

Even the most casual observer will have noted that testing has become an increasingly prominent issue in the electronics industry in the past few years. Themes in professional testing circles have quickly evolved from "test" to "design for test" to "design and test." In fact, testing is now often in the critical path of new product realization and, in many cases, represents more than a third of the total product-realization cost.

Testing has become increasingly important due to two major drivers, one market based, the other technology based:

- First, due to global competition, customers demand greater product functionality, higher quality, lower cost, and improved ease-of-use in the products they buy.
- Second, the increasing level of silicon integration will continue through the rest of the 1990's, resulting in ever-increasing device speeds and greater packaging density of electronic products.

Both of these drivers have, in turn, resulted in increased cost and increased product-realization intervals, in part because of the traditional test approaches used in the product-realization process. Industry, government, and academia have responded in recent years to meet these challenges by developing new test approaches and technologies. In this issue, we describe some recent efforts within AT&T to develop and apply some of these new test technologies.

As indicated in Figure 1, testing permeates our product-realization process, and is a critical determinant of cost, quality, and interval. These new test approaches, and other test advances that will follow in future years, will provide such significant benefits as:

- Shorter time to market,
- Lower manufacturing cost,
- Reduced capital for test equipment,
- Reduced development cost,
- Improved out-of-the-box quality,
- Reduced field-installation time,
- Increased product up-time, and
- Reduced field-maintenance cost.

Product-realization teams that make early use and take full advantage of these new testing methods can create significant competitive advantages in the products they introduce into the marketplace. Hence, testing is no longer a technology of concern only to specialists—it is now a mainstream business factor for every manufacturer of electronic products who would hope to be competitive in today's global marketplace.

Why Test?

The long-standing conventional wisdom regarding testing, well articulated by Dr. W. Edwards Deming and his disciples, is that testing is a non-value-adding activity that we should strive to minimize in our product-realization process. The notion is that by investing our efforts in continuously improving our processes, we can more cost effectively reach a required level of quality than by "screening in" quality via testing.

But the validity of this idea depends greatly on certain key parameters of the problem, specifically:

- What are the process capabilities of our product-realization processes?
- How much can these capabilities be improved, and at what cost?
- What capabilities must these processes have for us to continue to be successful in the marketplace?

Panel 1. Acronyms Used in This Paper

ANSI — American National Standards Institute
BIST — Built-in self-test
DFT — Design for testability
IC — Integrated circuit
SMT — Surface-mount technology

In considering these questions, the traditional focus has been on *manufacturing* processes. The options for improvement have focused on improving manufacturing process control to minimize process variability and, thereby, drive the actual process to its capability limit.

There's more to product realization than manufacturing, but let's stick with manufacturing for a moment. What if the capability of our manufacturing process is less than what's required to deliver an acceptably high-quality product to customers? In such a case, clearly we must "screen in" quality via end-of-line testing, even as we urgently seek ways of improving process capability.

Alas, it's much easier for customers to establish ever-more stringent quality requirements than it is for us to find ways to improve process capabilities to meet them. In fact, given any arbitrarily good but less than perfect process, our customers can easily establish a quality requirement that exceeds our process capability, thus establishing parameters on the problem that require us to "screen in" quality via testing.

There is, of course, an added cost for screening product at the end of a manufacturing line. Most customers will moderate their quality demands in recognition of what it actually would cost to meet them. But they will set cost/quality expectations based on what globally optimized, well-controlled manufacturing processes can deliver. So, to be successful, we must:

- Establish and maintain a product-realization process that has a process-capability that is consistent, in terms of quality and cost, with what leading-edge technology can deliver;
- Apply appropriate process-control techniques to assure that our processes are, in fact, operating near their process capability; and
- Incorporate some amount of testing to achieve a level of quality in excess of what our process capability provides—a quality level typically required by a large subset of our customers.

This last requirement will stay with us, even as we continually improve our process capability to ever higher quality levels. Until we are able to drive our process capability and process-control mechanisms to virtual perfection, we will always need to test. As new product requirements continually fuel the creation of new, technology-stretching manufacturing processes, we have an unending supply of imperfect processes to improve.

What's Different Now?

As a practical matter, we typically look at how far our end-of-line product quality falls short of the quality required by the majority of our customers, then focus our process improvement efforts accordingly.

This strategy has, in recent years, led to a new paradigm for testing in an environment of:

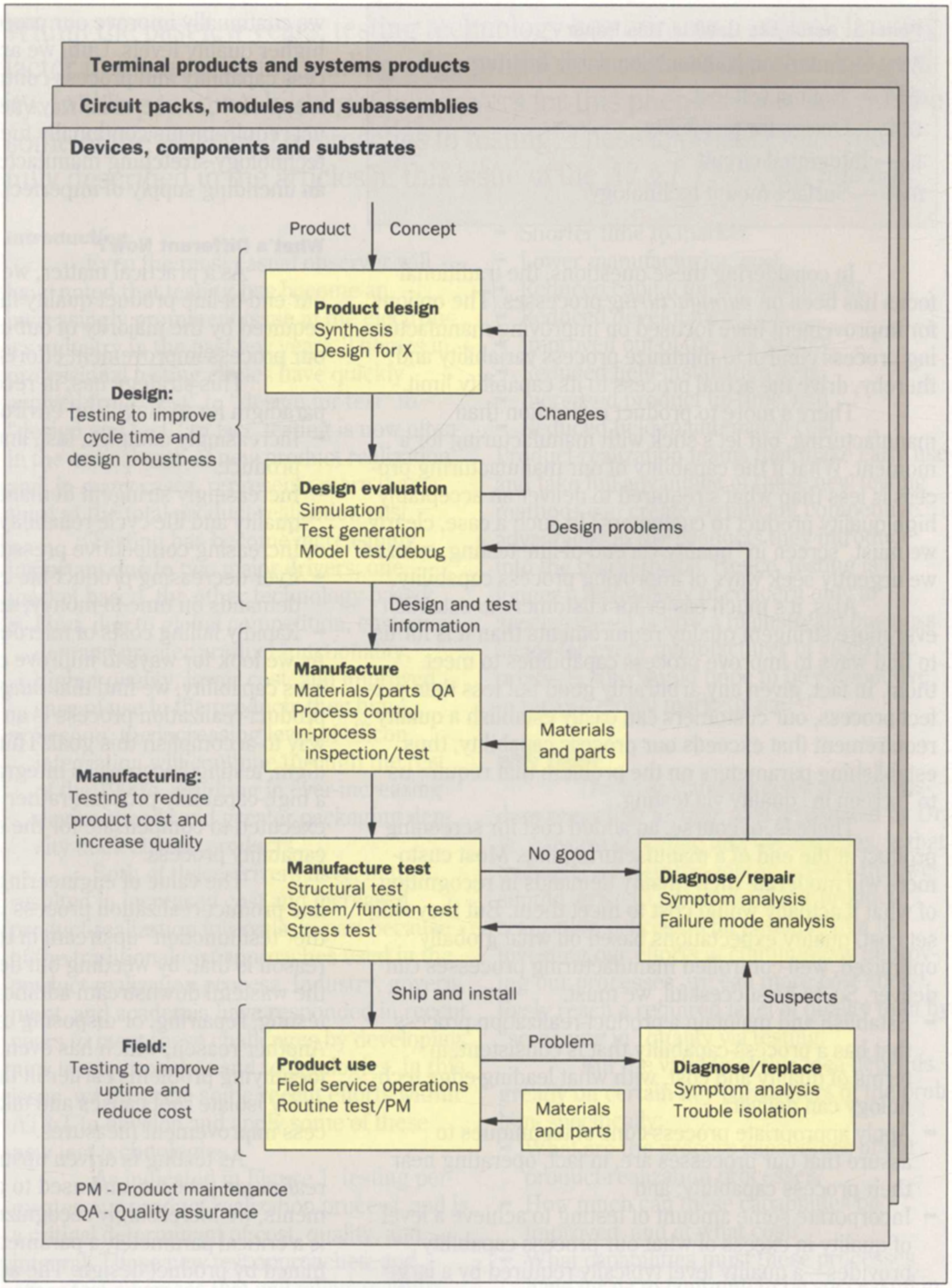
- Increasingly complex, fast, and densely packaged product;
- Increasingly stringent demands for out-of-the-box quality and life-cycle reliability;
- Increasing competitive pressure on costs;
- Ever decreasing product life cycles and corresponding demands on time-to-money; and
- Rapidly falling costs of microelectronics circuitry.

As we look for ways to improve our manufacturing process capability, we find that *integrating* testing into the product-realization process is an extremely powerful way to accomplish this goal. Thus, in the new paradigm, testing becomes an integral, value-adding part of a high-capability process, rather than a "necessary evil" executed to compensate for the shortfalls of a low-capability process.

The value of engineering testing into the mainline product-realization process is magnified as we move the "test function" upstream in the process. One obvious reason is that, by weeding out defects early, we can avoid the wasteful downstream additional costs incurred by testing, repairing, or disposing of defective products. Another reason, which has even more impact, is that, by identifying problems earlier in the process, we can more easily isolate root causes and take the appropriate process improvement measures.

As testing is driven upstream in the product-realization process, and used to guide process improvements, we increasingly recognize that product testability is a critical parameter, a parameter that is basically determined by product design. The advantages to be derived from having easily testable, diagnosable product components and subsystems in downstream manufacturing

Figure 1. Testing permeates AT&T's product realization process, and has a major impact on product cost, quality, and time-to-money. In aggregate, test-related costs for today's electronic products typically range from 30% to 50%. Moreover, the increasing level of product integration and packaging density is outstripping the capabilities of traditional test methods. The result: new test methods are being aggressively developed and rapidly deployed into our product design, manufacturing, and field operations. These new methods can be used for developing a wide range of products, including devices, components, and substrates; circuit packs, modules, and subassemblies; terminal products and systems products.



processes are so significant that we can afford to make an incremental investment in the product design to facilitate this testability.

How much of an investment can we afford to make in improving product testability? Clearly, the key factor is the savings we can make in downstream processes by using this improved testability to identify defective products, and to provide the insight necessary to develop process improvements. But, in looking downstream, we must look beyond the manufacturing floor. Our products go into customer environments. Coping with failures in those environments can be greatly facilitated by the extent to which testability has been designed into the product.

Our consideration of product testability has to be made in the context of testing methodology. For example, the design of a testable circuit pack, which is intended to be tested by traditional in-circuit test equipment, will include a full complement of test pads. These pads allow the tester to mechanically contact internal nodes and exert control and observation signals. If the product's density precludes incorporating these access points, we must invent other testing methods, and direct our product-testability enhancements to these methods.

It is exactly this consideration of packaging density that provided initial impetus to the development of boundary scan technology. Boundary scan is now both an IEEE and ANSI standard. More importantly, it is perhaps the fastest standard to move from proposal to widespread adoption in the history of IEEE standards. Clearly, there must be a significant value-added here. Yau et al.[1] provide further details on this rapid evolution of boundary-scan technology, both in the industry at large and within AT&T.

The revolutionary increase in complexity and speed of microelectronics products has provided much of the challenge for testing. For one thing, traditional probe-based testing methodologies have definite limitations in the speed at which they can drive these devices over multiple centimeters of interconnect. For another, unless special provisions are made in the design, a very large scale integration (VLSI) device typically provides very little controllability and observability of its internals via its externally accessible inputs and outputs. Controllability and observability are key determinants of how difficult it is to thoroughly test a complex product.

Fortunately, although the difficulty of testing microelectronics products has increased, the cost of embedding testability enhancements has decreased. Hence, we have reached an economic tradeoff point where, for many applications, it is justifiable to incrementally invest as much as 30% to 40% in embedded electronics to improve testability. In fact, design for testability (DFT) has become a hallmark of modern microelectronics design methodology in the digital domain. Crane et al.[2] outline the major factors that are driving this trend, and test issues and challenges deriving therefrom.

Design for testability methods can be extended in concept to built-in self-test (BIST). In effect, the product becomes so "testable" that it can effectively test itself! This concept has, in fact, been reduced to practice in many of AT&T's digital integrated circuits (ICs). Agrawal et al.[3] outline the methodologies and tools that AT&T has developed to support the BIST paradigm.

While built-in self-test is conceptually attractive, in practice there are limits to the level of thoroughness of testing that BIST can accomplish with acceptable incremental cost. Hence, there remains a considerable need for testing digital devices using external-testing resources. This, in turn, motivates the need for automatically generating a suite of tests that can be applied by an external tester to thoroughly test a given digital device.

The computational difficulty of such test generation is heavily dependent on the level of testability of the circuit. Thus, the test generator can be used to aid in highlighting testability problems. Since the test generator needs to have access to the circuit design in electronic form, it is also the ideal tool to help designers improve the product testability by adding appropriate test structures. Chakraborty et al.[4] describe several of the technical challenges involved, and outline how these were dealt with in creating the GENTEST generator, a tool developed within AT&T to provide such capabilities.

What About Analog?

The application of DFT methods, extending all the way to built-in self-test, has been primarily in the *digital* domain. Is this because digital circuitry is inherently simpler to test? Certainly, the methodology we use to test digital circuits is in some sense simpler, primarily because test engineers have adopted a relatively tractable "stuck-at" fault model to measure the quality of testing. The premise of the "stuck-at" fault model is that any product defect will exhibit a "stuck-at" symptom when an appropriate sequence of test inputs is applied. The "stuck-at" symptom is that which would appear if a gate-level node of the circuit were permanently forced to a logical "0" or a logical "1" state. Using DFT techniques, we can design test suites for "real-life" digital products that provide virtually 100% coverage for all "testable stuck-at" faults.

While "100%" seems attractive, it's important to take note of the qualifiers. There are some potential gate nodes whose hypothetical stuck-at "0" or "1" condition cannot be detected by *any* sequence of tests. This condition can be introduced, for example, by redundant-circuit design. Such "untestable," stuck-at faults are usually identified by design-for-testability (DFT) tools, such as the GENTEST generator, but often are excluded from the fault-coverage metric. For some digital designs, "untestable stuck-at" faults can be 20% or more of the total number of faults.

Beyond the question of "untestable" faults is that of the validity of the stuck-at fault symptom in representing all important product defects. Many well-known defect mechanisms in fact *do not* exhibit "stuck-at" symptoms. Often, they can cause marginal, or intermittent, circuit operation. Sometimes, their effect is to reduce the lifecycle reliability of the product.

As we get better at dealing with the "easy" stuck-at faults in digital circuits, the relative importance of faults that cause marginal or intermittent problems increases. One approach to this problem is to extend the fault model and DFT methods within the digital domain. Considerable work is ongoing, for example, to model "delay faults" in digital circuits.

Another approach is to examine analog parameters and operational properties of the circuit. Traditional analog testing, dating back to the pre-digital era, relied heavily on this approach. With today's increasing proportion of digital content in analog products, there are opportunities to adopt novel methods for such analog testing. Lopresti et al.[5] describe and compare methods that can be used to test such digital-analog products.

Yet another approach to dealing with the fundamentally analog nature of electronic circuits is to seek to more directly expose defects by inspecting the materials that comprise the product before and during the process of manufacture. (For some purposes, testing is defined as confirming the proper electronic operation of a circuit, and is distinguished from inspection, which seeks to indentify product flaws without electrically operating them. For purposes of this discussion, both of these approaches are included in the generalized notion of testing).

Carver et al.[6] outline how novel optical techniques can be used to characterize the quality of semiconductor materials used to fabricate the electronic devices that are at the heart of our complex systems.

Any concept of product quality must factor in the intended operating environment for the product. Considerations of test thoroughness must include these environmental variabilities. Chan et al.[7] outline stress-test methodologies aimed at identifying product problems that are sensitive to these environmental factors.

Design-for-test is of limited value if the capabilities it provides are not exploited in the testing operation itself. Much of this testing activity occurs on the manufacturing floor, where we must assimilate new testing methods into an existing infrastructure of processes, people, and equipment. Hence, a very vital concern is assuring that the nuts-and-bolts problems of manufacturing testing are addressed as we move new testing capabilities into practice. Allen et al.[8] outline the evolution of test-related processes in the manufacturing of high-density circuit packs, using surface-mount technology (SMT) at one of AT&T's manufacturing plants, as new test methods have been introduced.

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A common thread through all of these developments is that testing technology has become intertwined with product and process technology, and this coupling is growing ever tighter. If testing ever really was a low value-adding "necessary evil," to be minimized or eliminated, that time has passed. Strategies for testing are now as important to product managers and marketers as they are to engineers and developers. The "right" testing strategies translate into competitive strength in basic success factors: cost, quality, and time to market.

In the context of successful product realization, testing has clearly gone critical path.

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