Boundary-Scan Testing for Electronic Subassemblies and Systems

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Since 1990, an important change in electronic design and test methodologies has been under way. The change is facilitated by ANSI/IEEE 1149.1, which is known as the Test-Access Port and Boundary-Scan Architecture standard. AT&T Bell Laboratories played a major role in the promulgation of this standard, and AT&T design and manufacturing engineers have been implementing its provisions for several years. This paper reports on the ways in which the standard has been employed in developing AT&T products, the benefits that have been achieved, and the future opportunities available using the technology it details.

Introduction

There exists a challenge of testing in the product-realization process (PRP), which is defined as the development, building, and maintenance of products. The PRP ranges in scope from the definition of customer requirements, specification of product architecture, and the design of system functions, to the decomposition of the design into a hierarchy of interconnected units. The PRP continues with the building and "debugging" of first models, to the verification that the design meets stated requirements. The focus of the PRP then shifts to manufacturing, where products are fabricated, assembled, and interconnected into systems for delivery to customers. The PRP also includes field maintenance, ensuring that customer requirements are met throughout a system's life cycle.

Although progress in structured design techniques and automation have minimized process errors, defects can occur during design and manufacturing, and service disruptions are still possible due to system failures. Testing identifies failed units and isolates the causes of failure in repairable units. The better the ability to diagnose product difficulties, the more likely that downtime will be short and that failure-mode analysis (FMA) will lead expeditiously to constantly improving quality.

Test development can be time consuming. Tests are required for each level of the assembly hierarchy—chip, multichip module (MCM), board, subsystem, and system—and for installation and servicing.

In recent years, board testing required access to all circuit nodes on the printed wiring board (PWB). Access was gained by means of spring-loaded nails built into a complex test fixture. The test fixture was mounted on automatic test equipment (ATE), known as an in-circuit tester. Once again, the methodology was completely limited to only one level of the assembly hierarchy. Moreover, because ATE tests required a significant amount of time and money to develop, they were seldom used to debug initial models. As a result, valuable development time was spent manually correcting defects due to manufacturing problems, instead of proving-in the product at the design stage. High-density interconnecting and packaging, such as the chip-on-board and dual-sided surface-mount techniques, have made in-circuit testing (ICT) a very difficult methodology to implement.

In system testing, the general rule was to rely on complex software programs to diagnose and verify system functionality. These programs could not always locate and define a circuit-pack-level fault with the desired accuracy. None of the effort on lower-level test development was reused.

In order to address some of these issues and concerns, the ANSI/IEEE Standard 1149.1, Test-Access Port and Boundary-Scan Architecture, was promulgated.[1]

Panel 1. Abbreviations, Acronyms, and Terms

ANSI/IEEE 1149.1 — the Test-Access Port and Boundary-Scan Architecture standard, which details specific and recent changes in electronic design and test methodologies
ATE — automatic test equipment
BIST — built-in self-test
BSR — boundary-scan register
DFT — design for test
DSP — digital signal processor
EST — environmental stress testing
FMA — failure-mode analysis
FRU — field-replaceable unit
IC — integrated circuit
ICT — in-circuit testing
I/O — input/output
MCM — multichip module
PRP — product-realization process
PWB — printed wiring board
scratch probing — a test method in which a fine probe is scratched along the side of a device in an attempt to isolate defects to a pin
TAP — test-access port

Introducing Boundary-Scan Architecture

Conceptually, boundary-scan architecture, shown in Figure 1, is quite simple. At the integrated-circuit (IC) level, it is a collection of test circuitry consisting of:

- A test-access port (TAP), comprised of four or (optionally) five pins on a chip, which includes the serial data input (TDI) and output (TDO) pins, a dedicated test-clock pin (TCK), a control pin (TMS), and an optional pin that resets the test logic of the device (TRST).
- A protocol for communicating with the test logic over the TAP.
- A group of shift registers (Figure 2), connected in parallel between the test-data input/output (I/O) and a control mechanism for selecting the active register.

At the board level, the simplicity of the concept continues, as shown in Figure 3. TCK, TMS, and TRST are broadcast to all boundary-scan ICs. TDO of one chip's TAP is connected to the TDI of another chip's TAP, so that a chain is formed. In the simplest approach, the TAP leads appear at the board edge. The power of the boundary-scan architecture is that a standard interface is available for testing at the chip, board, and system levels. With this simple structure, a wide range of test and nontest functions is available. ICs from different vendors can be utilized, cooperatively, to achieve a test objective at any level of a product's hierarchy.

Figure 2 shows the device logic that the standard mandates. Three of the parallel registers have mandated forms and functions. The single-bit bypass register provides a short cut through a device, so that the number of cells in the board-level boundary-scan chain can be minimized to optimize test throughput.

The instruction register provides the means for selecting the active register between TDI and TDO. It can also initiate self-test, a capability that is widely used within AT&T. Finally, the register can also extend the ANSI/IEEE standard for user-defined functions.

The boundary-scan register (BSR) provides controllability and observability at an IC's signal I/O. This controllability and observability is used to test the interconnect at the board/module level.

ANSI/IEEE standard 1149.1 defines other optional functions to aid in device identification, as well as ICT and cluster testing. The standard can also support in-circuit emulation and other nontest functions.[1,2]

Common DFT Framework for End-to-End Testing

With the boundary-scan standard, there is now a unifying design-for-test (DFT) framework for controlling end-to-end design and testing costs along two orthogonal dimensions: *space*, defined as the assembly hierarchy shown in Figure 4; and *time*, defined as the product life cycle. This section briefly discusses the merits of the boundary-scan architecture, as a new DFT framework, from the perspectives of these two dimensions.

Assembly-Hierarchy Perspective. Boundary-scan testing can help realize significant cost savings across all three product-assembly levels: device, circuit-pack, and system. Compared to traditional *ad hoc* DFT techniques, boundary-scan testing offers three important advantages:

- The boundary-scan architecture and TAP provide a standard gateway for accessing test resources throughout the assembly hierarchy. For instance, the circuitry for interconnect testing can be accessed as easily at the board level as at the system level, with minimal hardware overhead. The same is true for

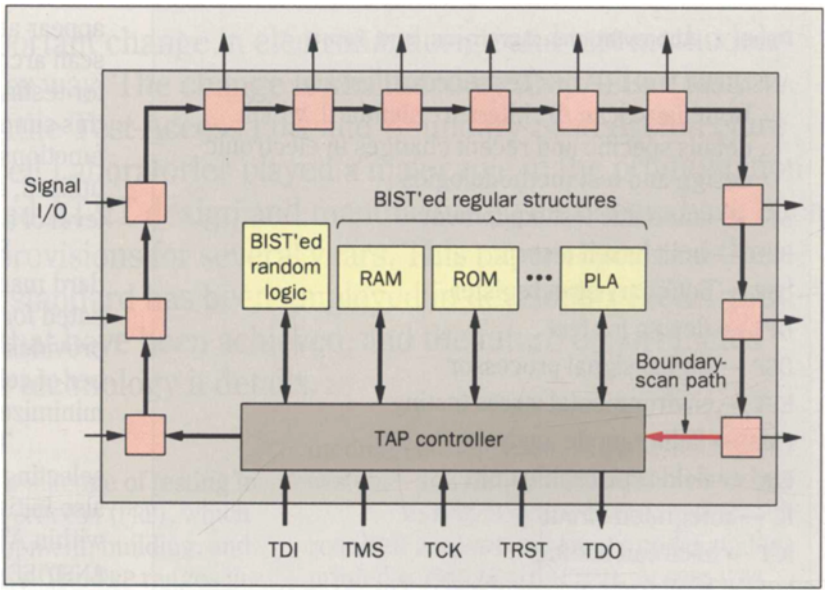

Figure 1. This drawing depicts a boundary-scan device. It has four additional pins (TDI, TDO, TMS, and TCK) that are required by the ANSI/IEEE 1149.1 standard, and an optional fifth pin, TRST. It also includes some testability logic. The device's core logic is self testing. It has been partitioned into regular structures and random logic. Each logic block has been made self testing, using techniques specific to their structure. Control and access is by means of the TAP. As a result, the testability features within the device can be reused at all levels of the product hierarchy.

built-in self-test (BIST) circuitry.

- Greater diagnostic accuracy at the board-test level results in fewer inaccurate device tests. Sometimes, good devices are removed and discarded simply because they are not soldered correctly to a PWB. As device complexity and cost continue to increase, diagnostic accuracy becomes more important.
- DFT circuitry and test vectors developed at one level of assembly can be reused at another level, thereby reducing total product cost.

Product Life-Cycle Perspective. Boundary scan can play a major role in reducing the total interval for designing and testing within the PRP, resulting in faster time-to-market. Boundary scan contributes significantly to shortening the design-and-test interval by:

- Facilitating implementation as a simple, standard framework for designing an up-front DFT architecture. This avoids many potential test-related problems, where the time interval required for correction would be too long and the cost too high.
- Supporting the concept of concurrent engineering, which merges two traditionally separate and sequential processes—designing and testing—into a tightly integrated process. For example, while the boundary-scan architecture can greatly simplify production testing, it can also support such non-test-related activities as in-circuit emulation and first-model debugging.
- Reducing the tendency to "reinvent the wheel." The standard DFT framework, based on boundary-scan architecture, encourages extensive reuse of proven and effective DFT concepts, algorithms, and circuit blocks. Such reuse provides additional time for designers and test engineers to meet product-specific challenges. The design methodology for boundary-scan cells is relatively mature, as is the design of the boundary-scan/BIST interface. Tools now exist for the automatic insertion of boundary-scan circuitry into a pre-existing logic design. And, AT&T Tapdance® software provides a thorough check on a logic design's conformance to the ANSI/IEEE standard.
- Automating test-program generation and test-information transfer across the design-to-manufacture boundary, which results from standardization. The extensive use of test-automation tools can reduce test-development time by two orders of magnitude. Such tools also minimize the probability of errors that can be introduced by manual testing, especially at the stages of new-product introduction or design-to-manufacture hand-off. Tools for automatic generation of complete, board-level, boundary-scan-based tests are available from multiple vendors. Also, an appendix to the ANSI/IEEE standard is now being developed. It provides a common language for transferring the description of a device's boundary-scan circuitry between automated design and testing tools. The appendix should be completed and available soon.

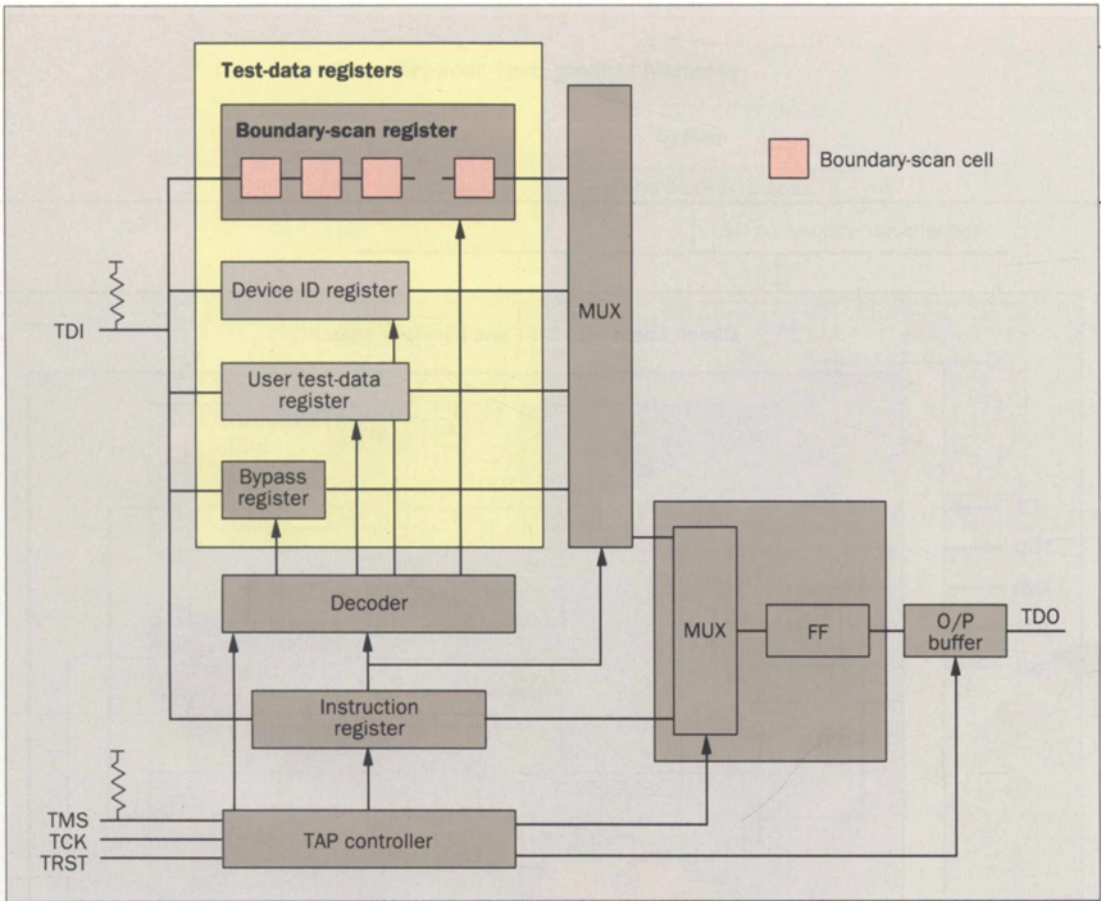

Figure 2. This illustration shows the logic that must be included in each device in order for the device to claim conformance. The TAP controller is a 16-state, finite-state machine that controls the operation of the test logic synchronously with TCK. The instruction register determines the register that is connected between TDI and TDO. Boundary scan is the key register in this architecture, providing direct controllability and observability over the entire signal I/O. The one-bit bypass register is used to "short-circuit" a device and reduce the length of a board-level boundary-scan chain, thereby optimizing test throughput. The optional device ID register identifies the device's function and manufacturer. User-defined registers can extend the architecture into other applications, such as in-circuit emulation.

Application Across the PRP

The Test-Access Port and Boundary-Scan Architecture standard, ANSI/IEEE 1149.1, can be applied to the PRP at five levels or stages. Brief discussions of each of these levels follow.

Device Test. At the device level, boundary-scan architecture provides a serial channel for accessing the internal logic of a device, for both test and nontest purposes. The most significant contribution that boundary-scan architecture has made in this area is the definition of the optional RUNBIST instruction, which is a standardized method for initiating BIST within a device and obtaining its result. The TAP can also be used to access other device-test features, such as internal scan chains. Devices in several major products, produced by the AT&T Transmission and Switching Systems divisions, have RUNBIST-compatible BIST.

A boundary-scan device can be used to simplify functional testing. Its ability to access internal, user-defined registers also serves several other purposes—including initializing complex, finite-state machines and internal memory. Furthermore, boundary-scan access can be extended to provide complete in-circuit emulation capability, which is the approach taken by the DSP16XX family of AT&T digital signal processors (DSPs).

Many interesting applications of the boundary-scan architecture remain to be explored. The BSR can be used to partition the testing of digital and analog portions, using traditional test approaches, rather than testing a mixed-signal device as one large circuit. For MCMs, boundary-scan testing can be used to verify the alignment and bonding of device I/O pads to substrates. The ANSI/IEEE boundary-scan standard also provides a simple mechanism to check a device's immunity to simultaneous switching of I/O buffers, and for measuring I/O speed characteristics.

Lab Debugging. Users report that a major advantage of the boundary-scan architecture is the dramatic reduction of time required for proving-in first models in the laboratory. There are several reasons for this. As discussed earlier, AT&T DSPs have extensive, in-circuit

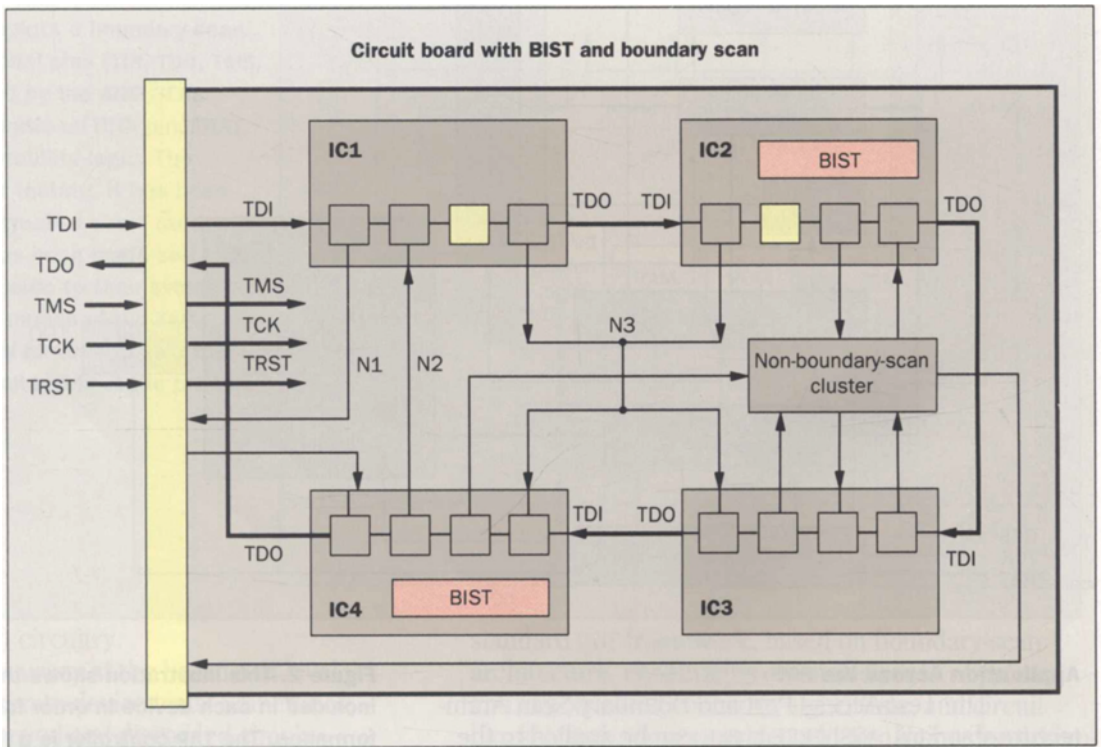

Figure 3. A typical application of boundary scan at the board level is shown. A realistic scenario is depicted where there are both boundary-scan and non-boundary-scan devices. Starting from the edge of the board TDO, one device is connected to the TDI of the next board, until all the devices are connected in a daisy chain. TMS, TCK, and TRST are broadcast to all the devices. At the board level, boundary scan can be used to test all the nets of type N1, N2, and N3 without any in-circuit access. Non-boundary-scan devices require either ICT access or testing as a cluster, using the boundary-scan access provided by the neighboring devices. Finally, devices that have BIST controlled by means of the TAP can be easily tested by invoking the self-test function and scanning the signature.

emulation capabilities, which are accessible via the TAP. This feature can be used to develop and debug an application very quickly. Also, the functional test support that boundary-scan architecture provides can be used to accelerate design validation. Finally, a boundary-scan device can be used to ensure that the structural integrity of a circuit pack is not compromised as it goes through the modifications that are an inevitable part of debug-and-design prove-in.

Another potential laboratory application of the boundary-scan architecture is ensuring that a design is robust. This is accomplished by providing the means for extensive model operation and testing under environmental stresses. The operating and testing parameters can also be reused for environmental stress testing during manufacture. The laboratory application of boundary scan is currently being refined and implemented, on a prototype basis, for some AT&T products.

Factory Test Development and Application. Separation of function from structure is one of the most important contributions of boundary scan. This permits development of testing without regard to the function of a unit under test, which can greatly accelerate prove-in and test development through extensive automation.

For a system having a boundary-scan device, test development can begin as soon as design data is available. There is no need to wait for the development of model devices and circuit packs, and no need to rely on device-level functional tests with complex timing. As soon as the first models are available, test prove-in can typically be completed in hours or days—as opposed to the several

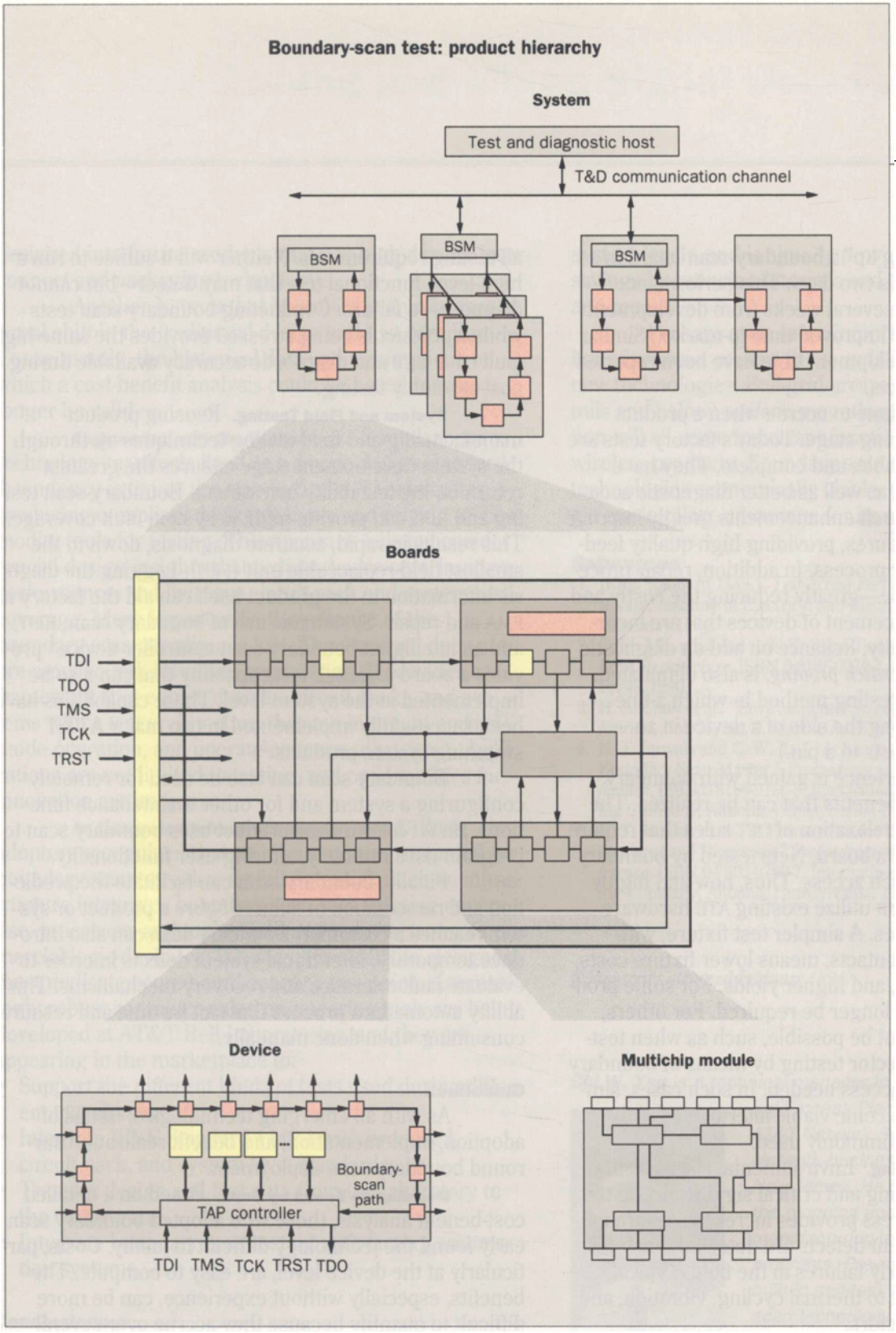

Figure 4. This diagram depicts a typical assembly hierarchy of a product. Devices, multichip modules, boards, and systems are illustrated. Boundary scan can be used as the basis for a test-and-diagnosis architecture that ensures test reuse, high fault coverage, and diagnostic accuracy and resolution at each level in the product hierarchy. This approach ensures maximum return on investment in testing, because the pay-back occurs at each level in the PRP and over the product's life cycle.

weeks required prior to implementation of the ANSI/IEEE standard. The shortened prove-in interval allows a model shop or factory to have fully tested first models in the hands of design engineers—ready to begin design validation—within one to two days of assembly.

The Head-Start Program at the AT&T Global Information Solutions division in Columbia, North Carolina, strives for a 48-hour interval. The average time

now required to "bring up" a boundary-scan board in a major AT&T product is two days. This performance improvement has cut several weeks from development schedules and greatly improved time-to-market. Similar reductions in test development time have been reported in other AT&T products.

Benefits continue to accrue when a product enters the manufacturing stage. Today's factory tests are now more robust, reliable, and complete. They have higher fault coverage, as well as better diagnostic accuracy and resolution. Such enhancements greatly improve repair and FMA procedures, providing high-quality feedback for the assembly process. In addition, repair procedures are more precise—greatly reducing the costly and time-consuming replacement of devices that are incorrectly identified as faulty. Reliance on add-on diagnostic techniques, such as *scratch probing*, is also eliminated. (Scratch probing is a testing method in which a fine probe is scratched along the side of a device in an attempt to isolate defects to a pin.)

As more experience is gained with boundary scan, there are other benefits that can be realized. The most important is the relaxation of DFT rules that require access to every net on a board. Nets tested by boundary scan need not have such access. Thus, new and highly integrated products can utilize existing ATE hardware without costly upgrades. A simpler test fixture, with fewer spring-loaded contacts, means lower fixture costs, reduced maintenance, and higher yields. For some products, a fixture may no longer be required. For others, use of a fixture may not be possible, such as when testing MCMs. Edge-connector testing by means of boundary scan provides all the access needed. In such cases, simple, low-cost testers become viable alternatives to the capital-intensive ATE commonly used.

Reliability Testing. Environmental stress testing (EST) is a tool of growing and critical significance to the PRP. Testing under stress provides increased assurance that products with latent defects are detected. Such testing helps eliminate early failures in the field. Typically, EST subjects a product to thermal cycling, vibration, and other crucial stress factors.[3]

One problem with EST is that defects detected when a product is thermally stressed will not be detected at room temperature. Simply stressing a product thermally and retesting it at room temperature will not satisfy all testing requirements. Neither will it suffice to run a high-level, functional test that may detect—but cannot diagnose—a failure. Conducting boundary-scan tests while a product is being stressed provides the same high fault coverage and diagnostic accuracy available during post-assembly testing.

System and Field Testing. Reusing product-manufacturing and field-testing techniques up through the system-development stage ensures the greatest return on the testability investment. Boundary-scan testing and BIST can provide high, in-system fault coverage. This results in rapid, accurate diagnosis, down to the smallest field-replaceable unit (FRU). Logging the diagnosis information in the product itself can aid the factory in FMA and repair. Systematic use of boundary scan, BIST, and an intelligent boundary-scan controller device[4] provides a board-level self-test capability that can also be implemented at the system level. These capabilities have been successfully implemented in two major AT&T switching-system products.[5]

Boundary scan can also be used for remotely configuring a system and for other maintenance functions. An AT&T wireless product uses boundary scan to program DSPs remotely, altering user functionality.

Finally, boundary scan can facilitate the prediction and remediation of failures *before* a product or system reaches a customer. Boundary scan can also introduce temporary, intentional system defects in order to evaluate fault-tolerance and recovery mechanisms. This ability automates a process that can be time and resource consuming when done manually.

Guidelines

As with all emerging technologies, issues of adoption, implementation, and benefit realization surround boundary-scan deployment.

Deciding on Boundary Scan. Based on a detailed cost-benefit analysis, those who adopted boundary scan early found the technology difficult to justify. Costs, particularly at the device level, are easy to compute. The benefits, especially without experience, can be more difficult to quantify because they accrue over several stages of the PRP and throughout a product's life cycle. According to managers of several early AT&T projects, boundary scan is an important technology today. Still, it is likely to become even more important tomorrow, when

designed into future products that use high-density interconnect and packaging technology.

Another issue is that boundary scan represents a real shift in the traditional design and test paradigm. Consequently, the historical data and assumptions on which a cost-benefit analysis could be based may no longer be valid.

Engineering with the Technology. Boundary-scan technology manifests itself as a device-design standard. A tendency is to use the standard as a "cookie cutter"—producing compliant device designs, and relying on commodity tools for testing. This approach fails to consider crucial design insights that reduce device cost, improve performance, and increase circuit-pack and system test coverage. More importantly, the essence of the boundary-scan paradigm is lost. The standard does not pre-empt sound, inventive engineering. It provides a framework that equips devices, circuit packs, and systems with a test architecture that can interrupt normal-mode operation, and operate concurrently with it. Applications are not limited to testing, and opportunities for innovation are immense.

An Integrated Infrastructure Is Evolving. Early adopters recognized that an infrastructure is needed for boundary scan to realize its full potential. Such an infrastructure integrates boundary scan with existing expertise, processes, and tools. Until a broad spectrum of commercial logic-device replacements is available, designers must dedicate some board space to test points. Increasingly robust computer-aided engineering tools are being developed at AT&T Bell Laboratories, and they are appearing in the marketplace to:

- Support the different kinds of tests used during different PRP phases;
- Integrate IEEE Standard 1149.1 with proposed, circuit-pack, and system-level standards;
- Transfer design and test data from the laboratory to the factory; and,
- Integrate boundary-scan testing with factory automation systems.

Conclusions

Boundary-scan technology offers significant advantages throughout the PRP. It increases overall quality, reduces costs, and shortens time-to-market. Boundary scan has applications at the device, board, and system levels, and is already providing significant savings by reducing intervals and eliminating rework and repair.

Perhaps even more important is the fact that boundary scan creates the foundation on which to build new technologies. Ball-grid arrays, MCMs, fine-pitch (15 mils and below) surface mounting, and microminiaturization will all serve important functions in next-generation wireless products. Boundary scan will help make these technologies economically viable, thus creating a strategic marketplace advantage for its users.

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