Ensuring Structural Testability of High-Density SMT Circuit Packs

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This paper overviews a "next generation," end-to-end realization process for circuit packs that enables reliable test access for structural testing of aggressive, surface-mount technology (SMT) designs. New test-access alternatives, such as boundary scan (B-S) and new fixturing techniques, are reviewed. Each stage of the process is examined relative to how final testability can be influenced. An overview of the software systems and features needed to support this process, including computer-aided engineering/computer-aided design (CAE/CAD) tools, boundary scan tools, and manufacturing/test data management systems, are presented.

Introduction

During the early 1980's, the process of designing tests for circuit packs (CPs) experienced a metamorphosis. The practice of designing a product and then "handing it over the wall," for testing by manufacturing test engineers, was being challenged. Both CP design and manufacturing engineers realized that testing needed to move from a reaction mode, designing testing techniques in the factory, to an interaction mode, where testing issues are included in the design phase. This change was brought about both by the needs of the business and by the explosive increases in circuit pack density.

Over the past 15 years, with the application of surface-mount technology (SMT), the density of CPs has more than quadrupled, including fine-pitch and very-fine-pitch SMT. This exemplifies how complex and dense designs have become, and the challenge that lies ahead for structural testing.

Until the early 1980's, the majority of circuit pack testing was performed on functional test systems, in which physical access was achieved through the circuit pack's edge connector (that is, the part of the circuit pack that connects to the back plane), and the quality of the pack was assured when the pack functioned properly. As the density and complexity of components increased, however, so did the cost of functional testing. The finer the SMT packaging geometries, the greater the chance for assembly defects, such as solder shorts and opens, misloaded components (either wrong components, improper mounting, or missing components), or electrically damaged components. Enter, then, in-circuit testing (ICT): a method used to verify the proper physical *structure* of assembled CPs using a rapid and accurate technique of fault isolation of all manufacturing defects.

Although automated test equipment (ATE) vendors offered ICT equipment in the early 1970's, the initial systems lacked the robustness required to test the most sophisticated digital circuits. It wasn't until the late 1970's and early 1980's that ICT systems began to offer a level of functionality that met or exceeded testing requirements. This enabled many AT&T manufacturing locations to implement test strategies based on ICT.

Design for In-Circuit Testability. The success of ICT relies heavily on the cooperation between design and manufacturing engineering. In ICT, testing each component while it is electrically isolated from other circuit elements removes many of the pitfalls of functional testing. The benefits of ICT, however, are weighed against the need to adhere to a specific set of design-for-testability (DFT) guidelines.[1] Two such guidelines are illustrated in Figure 1. For each node on the circuit pack, physical test access is required through a bed-of-nails (that is, a set of probes), along with the requirement that the test system must stimulate the device via a test signal input, and observe the response by the

device's output signal. These requirements are implemented during the circuit and layout design (when the physical attributes of the circuit are designed), thus becoming a part of the design.

For many years, the amount of CP real estate available for test access was not a significant issue. Designs had "inherent" DFT test access at the leads of through-hole mounted components—a condition not available in SMT.

Clearly, the proliferation of SMT and finer device-packaging geometries indicates it will not be possible in the future to support the current ICT access and controllability requirements without exhausting all test-access options. In a word, we're running out of space for physical access.

Advances in Structural Test Access

Traditional design-rule requirements for in-circuit testability call for at least one accessible test point, or probe site, for each signal net (a grouping of terminals of components that need to be interconnected). One such example is a through-hole lead, or test pad, for each signal net that can be accessed from the bottom side of the board. A distinction is made here between a via (a plated hole added to the board every time a printed wire needs to traverse to a different layer) and a test pad (a circular copper area specifically for test access). Almost without exception, the minimum probe-to-probe clearance requirement has been 100 mils. This conveniently aligns with earlier-generation circuit packs, which had been laid out on a 100-mil grid. In addition, test-probe suppliers offer robust, cost-effective probes that can be used within these geometric constraints.

With finer pitch, higher input/output (I/O) density, and SMT packages proliferating in new designs, layout grids must become more granular (50 mils) to make signal routing plausible. This need puts pressure on the 100-mil probe-to-probe clearance requirement and other design rules. Fortunately, new methods for circuit pack test access have surfaced to help relieve the situation.

Boundary Scan and Other Alternatives. In 1990, the IEEE approved and published the boundary scan (B-S) standard (IEEE Standard 1149.1-1990). This new test technique, developed to address high-density testing issues, offers a means to electronically access internal

test points of a circuit pack through its edge connector. Even though more boundary "scanable" digital devices are appearing in new designs, it is reasonable to assume that not all upcoming circuit packs will be fully testable with B-S, at least not for the next few years. Consequently, our next generation structural-test strategy and process should leverage whatever B-S capability is available to relieve the physical probing issues resulting from board real-estate constraints and automated test equipment resource limitations. We must also intelligently provide physical probe sites to ensure that complete structural-test coverage is achieved.

Figure 1. For each node on the circuit pack, physical test access is required through a bed-of-nails (that is, a set of probes), along with the requirement that the test system must stimulate the device via a test signal input, and observe the response by the device's output signal. These requirements are implemented during the circuit and layout design (schematic at bottom) when the physical attributes of the circuit are designed. The test requirements thus become a part of the design.
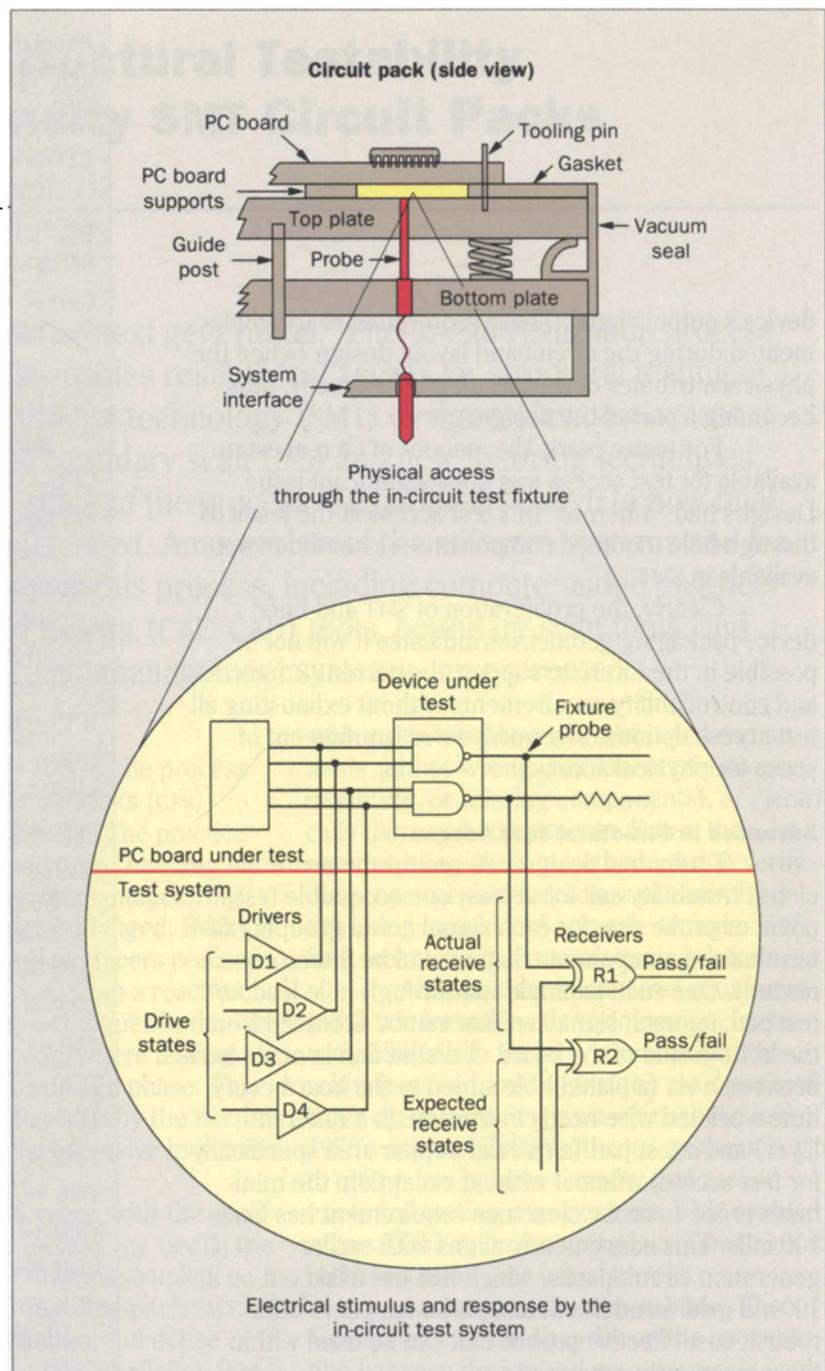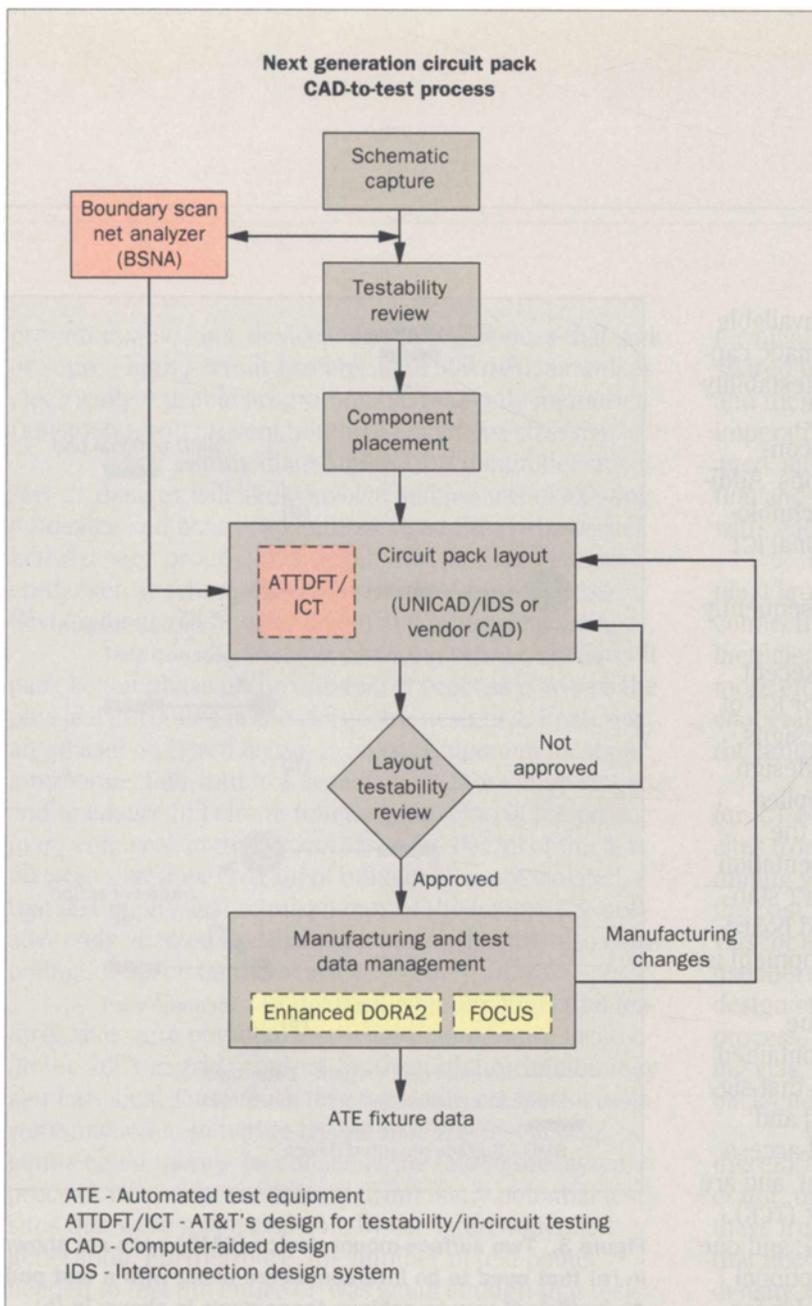
Recently, 75-mil probes have become an accepted alternative to 100-mil probes for very dense CP designs. While 50-mil probes have been available for several years, they have a track record of:

- High cost, in terms of piece-part costs and ongoing maintenance, and
- Unreliable contacting, including flimsy construction and low spring force.

We should keep in mind, however, that 100-mil probes are still preferred when layout and routing permit.

Innovations in fixture-fabrication (the manufacturing process for creating the physical test device) techniques have led to improvements in mechanical robustness and registration, as well as electrical performance. Requirements on test-target size may be reduced as a result, and finer probe sizes may be used with more confidence. A good example is TTI-Testron's new *Ultra-Lign* * probe and fixture technology.[2] More recently, impressive innovations, such as *TestJet* * from Hewlett-Packard,[3] and the *Safecracker* * Pattern Service from Teradyne,[4] offer alternative means to detect pin faults without requiring the generation and application of vectors (input patterns) to digital devices. These methods are particularly promising for application-specific integrated-

Next generation circuit pack CAD-to-test process

Schematic capture
→ Testability review
→ Component placement
→ Circuit pack layout (UNICAD/IDS or vendor CAD) [ATTDFT/ICT]
→ Layout testability review
  - Not approved
  - Approved
→ Manufacturing and test data management [Enhanced DORA2] [FOCUS]
  - Manufacturing changes
→ ATE fixture data

Boundary scan net analyzer (BSNA)

ATE - Automated test equipment
ATTDFT/ICT - AT&T's design for testability/in-circuit testing
CAD - Computer-aided design
IDS - Interconnection design system

Figure 2. Following schematic capture, testability review, and component placement of an integrated circuit, a suite of AT&T DFT tools is used for ICT (ATTDFT/ICT) to aid designers in choosing test sites from existing interconnection sites, and in determining when new test-access pads need to be created. The results of the ATTDFT/ICT process—the selected test points—are passed on to manufacturing by means of the AT&T software tools FOCUS and DORA2. The FOCUS tool provides an integrated software environment that manages circuit pack information spanning the product realization process (PRP) interval. The DORA2 tool is a UNIX-based system that translates AT&T circuit-testing information from the design to the manufacturing process.

circuit (ASIC) pin fault detection, but they also require physical nodal access.

Next Generation CP Design-To-Test Flow

To address the structural-testability challenges posed by high-density SMT circuit packs, an *SMT Circuit Pack Testability Team* was formed in AT&T in early 1992. Members included representatives of bare-board test, computer-aided-design (CAD) tool development, Network Systems test engineering, and layout-design organizations. At that time, the major topic of discussion was the current ICT design process, or processes, used in AT&T. Within this process, a new test design may occur at many points, from schematic capture through

manufacturing. In other words, the inclusion of test information in a CP design does not always occur at a specified point in time. Additionally, design data may progress via different computer-aided design, layout, and test-point selection tools, ultimately hampering the smooth transfer of design and test information.

Seeing the current and future structural-test needs of the new high-density CP designs described above, the SMT CP Testability Team formulated a new CAD-to-test process flow, shown in Figure 2, and specified that the next generation of CAD tool requirements should be able to use this new process. The principal feature of this process flow, which distinguishes it from the more traditional flow, is the early consideration of test information.

Specifically, decisions on how to best leverage available B-S resources are made immediately after schematic capture. Similarly, physical CP design rules for ICT testability can be considered in real time during CP layout.

The result is a process that maximizes concurrent engineering and reduces design iterations. Additionally, it blends the optimal use of new test technologies, such as B-S, more intelligently with traditional ICT design rules.

Each major stage of this process is subsequently described:

Structural Test Issues at Design Capture. Recent advances in SMT have created new challenges for ICT of high-density circuit packs. In complex digital designs, where testing problems are most difficult, new design techniques and testability standards must be applied early in the design process. The cooperation of the design community is essential for early implementation of the 1149.1 B-S standard techniques and the DFT standards for conventional circuitry[5,6] in device- and board-level designs. With such techniques, test development is simpler and more economical.

Boundary-Scan Testability. The B-S technique involves the inclusion of a shift-register stage contained in a B-S cell, adjacent to each component pin, so that signals at component boundaries can be controlled and observed using scan-testing principles. The test-access port (TAP) pins provide access to the component, and are composed of three input connections: test clock (TCK), test-mode select (TMS), and test data input (TDI); and one output connection, test data output (TDO). An optional fourth input connection, test reset (TRST), provides for asynchronous initialization of the test logic defined by the standard.

Once we have ICs with robust implementation of the 1149.1 standard, and the boundary scan description language (used to describe the features of a B-S device) has been certified, the DFT problems can be addressed at the board-level, schematic-capture phase. A simple board-level B-S "chain" has a single TCK and TMS signal broadcast to all the components involved in the test. The TDO signal of the first component to be tested becomes the TDI of the next component, and so on, until all components have been chained together.

To incorporate B-S at the board-level design, interfaces with conventional circuitry, mixed-logic families, and dynamic digital devices requiring quick refresh
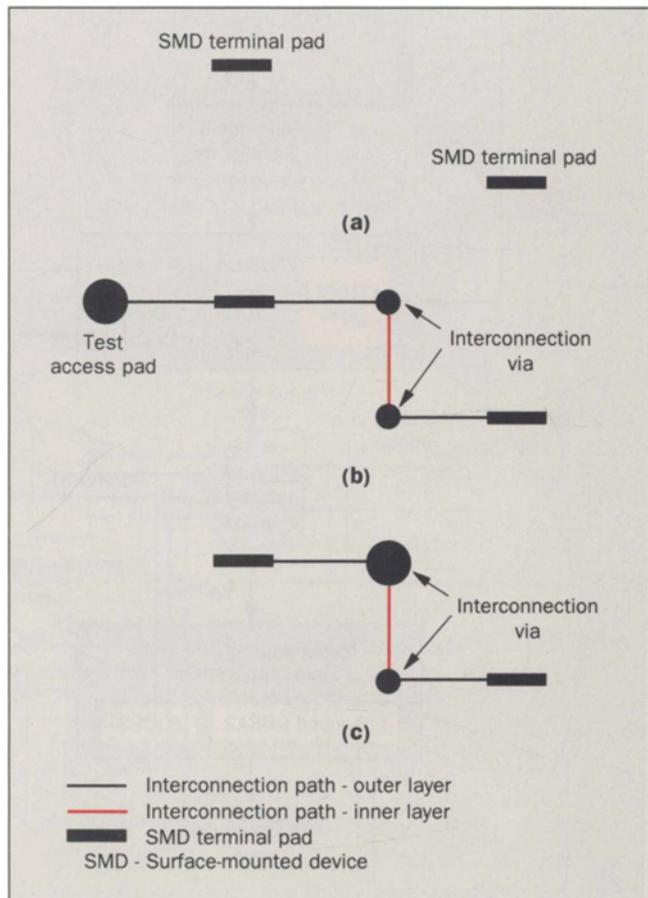
Figure 3. Two surface-mount device (SMD) pads are shown in (a) that need to be interconnected along with a test pad. An inefficient way to achieve these goals is shown in (b), while (c) shows a more efficient way to achieve these goals. The latter uses tools that cooperate with each other by making an optimal use of the limited space.

cycles must be considered. The technique of testing conventional circuitry through the boundary scan chain is known as Silicon Nails.[7]*

Beyond specific practices recommended for B-S implementation at schematic capture, adhering to DFT guidelines will make it simpler for ICT engineers, in the laboratories and in manufacturing, to develop testing. [1] These guidelines, not discussed at length here, would include handling clock signals by the ATE, including pull-up or pull-down resistors on device inputs (especially logic cell arrays), digital guarding, and instructions for

programmable logic devices. Tri-stating devices that sink or source high current (greater than 500 mA), as well as electrically erasable programmable read-only memories (EEPROMs), will prevent potential backdrive stresses.

For the immediate future, DFT in high-density SMT CP designs will likely involve making use of existing B-S-device and board capabilities. In addition, the earlier in the design process that testability issues are considered, even at schematic capture, the less painful test development will be after layout and in manufacturing.

Test Considerations at CP Layout Phase. The circuit pack layout phase of the CAD-to-test process is where the physical attributes of the circuit are designed. Features are placed on board layers to allow component location, interconnection, and test at various CP-fabrication stages, and to ensure full circuit functionality. One of the primary concerns in this process is to lay out all of the features so that their "region of influence" is not violated, that is, the physical requirements of the feature are not adversely affected by adjacent features that are also competing for space on the board.

Past Approach. In the past, all interconnection features that were potential test-access points were located on the 100-mil grid required for through-hole technology and bare-board test. With this approach, no special tools were needed to generate test points. The test-access points could merely be chosen at the end of the layout process, or even at the factory, from many potential test sites that were made available by the interconnection generation. Furthermore, the number of test points needed to test the entire CP was small enough that test-point density was rarely a concern.

SMT Impact and Up-Front ICT Generation. Now, however, the terminals of surface-mounted devices (SMD) are not accessible for testing, and do not fall on a 100-mil grid. Forcing vias on 100-mil grid no longer results in the smooth channels (straight "highways" allowed by routing interconnection) that previously simplified the interconnection process. Bare-board test no longer requires terminals and vias on a 100-mil grid. Finally, as a result of the high-density SMT, it is no longer affordable to make all interconnection vias large enough to automatically qualify as potential test-point sites, since they will reduce the space available for other interconnections. With component and board miniaturization has come an increasing demand for features, especially on the external layers. On the test-access side, the space not used by device

terminal pads and their region of influence must be shared by interconnection features and test-access pads, and their respective regions of influence. It is, therefore, imperative that the allocation of space be properly managed, and that the tools that generate the interconnection and test features complement, rather than compete with, each other for this space.

Figure 3 demonstrates this with a simple example. Figure 3a shows two SMD pads that need to be interconnected along with a test pad. Figure 3b shows an inefficient way to achieve these goals. Figure 3c shows a more efficient way to achieve these goals using tools that cooperate with each other by making an optimal use of the limited space.

A suite of AT&T DFT tools has been introduced for ICT (ATTDFT/ICT) to aid designers in choosing test sites from existing interconnection sites, and in determining when new test-access pads need to be created. In the past, either the designer used larger-than-necessary vias for all interconnections—at the expense of having to use more layers for interconnection—or a significant design effort was added at the "back end" of the layout process, either to add ICT access pads or to enlarge existing vias. As design density increases, however, this back-end approach will be totally untenable.

One of the major features of ATTDFT/ICT has, therefore, been an up-front ICT generator. With the generator, one can ensure that the needed test points are there from the start of the layout. If there are tradeoffs that need to be made in terms of clearance, test-point density, and the maximum number of test points handled by the test fixture, etc., they can be addressed up-front. Further, by having some familiarity with the interconnection goal, the ICT generator ensures that the test points it creates can also be used effectively by the interconnection tools that are applied later in the layout process. Once the test-access points are generated and approved, and the design is frozen from changes, one can begin the test-fixture generation process before the layout is complete.

Design Changes and Fixture Reuse. Due to circuit pack density and complexity, the cost of test fixtures (now ranging from $5,000 to $15,000) has increased. Thus, it is important that test-design tools aid the designer in making changes and in reusing the test fixture whenever possible, thereby saving both money and fabrication time. To this end, ATTDFT/ICT includes not only the capabilities to regenerate test points in

local areas that have undergone design changes, but also the ability to generate spare test points to help make the test fixture, when it is initially built, more adaptable to design changes.

Design Rules and Boundary Scan. For a CAD tool to be effective, it must capture and apply all of the design restrictions and tradeoffs that impact pertinent features, thus ensuring that:

- Features are designed right the first time,
- Any tradeoffs can be resolved up-front, and
- All features are verified before layout completion.

For ICT, design rules include clearances between test points, components, and board edge; component density; the distance from circuit drivers; and the maximum number of test channels available on the ATE being used. ATTDFT/ICT includes a set of design rules, as well as an interface to the B-S net analyzer (BSNA). This allows it to help the designer in choosing from different alternatives for test-point sizes, clearances, density, and test methods.

Generic Capability. As already mentioned, AT&T designers use a multiplicity of CAD tools in the layout of CPs. They also use a variety of tools, including several stand-alone, ad hoc, and often manually implemented tools, in test-point selection and test-fixture design. ATTDFT/ICT has been designed as a generic ICT design subsystem that executes in AT&T's internal UNICAD/IDS computer-aided design environment, as well as "on top of" vendor's CAD systems. This is made possible by a two-way interface that can be extended to communicate with any vendor CAD system. It takes ICT design features that are currently available in UNICAD/IDS, including the interface to FOCUS and DORA2 (two key internal AT&T systems supporting design transfer to manufacturing, and described below), and adds new features and the capability to handle new high-density SMT designs. Thus, it provides a single ICT design facility that can be used by all designers in AT&T, no matter which CAD system they are currently using or plan to use. Because it provides full functionality, as well as interfaces to CAD systems, BSNA, FOCUS, and DORA2, as shown in Figure 2, the CAD-to-test process is standardized and significantly streamlined.

Concurrent Team Development. ATTDFT/ICT is also available as a stand-alone system with a full or limited set of features. This allows the test engineer, test designer, and layout designer to work as a team, using their expertise to ensure that ICT features are designed optimally. For example, the test engineer could set up the design rules or verify their values before the beginning of the

design layout. The layout designer generates, selects, and audits the ICT test points. The test designer generates reports, plots, and other outputs, and transfers the needed design and test information through DORA2 for ATE circuit pack test design and fixture generation. Furthermore, by using the ATTDFT/ICT conferencing capability, team members who are not co-located can simultaneously view the process, observe the impact of design tradeoffs, then audit and finalize the accepted features on-line. This permits the final design to be approved by the entire team in real time.

Transferring Test Information to Manufacturing. The results of the ATTDFT/ICT process—the selected test points—are passed on to manufacturing by means of the AT&T software tools FOCUS and DORA2, shown in Figure 2. The FOCUS tool provides an integrated software environment that manages CP information spanning the product realization process (PRP) interval. The DORA2 tool is a UNIX-based* system that translates AT&T circuit-testing information from the design to the manufacturing process.

Traditionally, the test engineer working on a specified ATE would receive selected test points from DORA2. There was no defined process, however, to capture the final test points selected and reuse them for future artmaster revisions. (Artmaster is the creation of a photographic film of the circuit for etching.) With the ATTDFT/ICT enhancements to the FOCUS and DORA2 tools, test points selected by ATTDFT/ICT are preserved and migrated to the ATE. The final selected test-point information from the ATE is migrated back to ATTDFT/ICT to be used for future artmaster revisions.

The DORA2 algorithm and the test engineer will still be able to modify the selected test points, but now that information will be preserved for future artmaster revisions of that circuit. Existing test fixtures can be reused with modifications, thereby saving a considerable amount of money per artmaster revision.

FOCUS-Prime Description. As noted, the FOCUS-Prime[8,9] tool provides an integrated software environment that manages CP information spanning the product realization process interval, from early design-data acquisition to the definition and management of the CP assembly process. Within the FOCUS-Prime environment, design and factory personnel work cooperatively to acquire and correlate CP design data, create the requisite assembly processes, and transmit material-ordering information to a material-resource planning (MRP)

system. This results in a higher-quality product, realized in the least amount of time, at the lowest possible cost.

FOCUS-Prime In In-Circuit Test. The FOCUS-Prime role relative to in-circuit test begins with the acquisition of the physical and in-circuit probe data from a CAD workstation, and the correlation and verification of these objects with the product definition. These objects are then placed under version-and-change control, and are used by FOCUS-Prime to generate the ICT data file, called the universal DORA interface file (UDIF), for the DORA2 test system.

FOCUS-Prime will add new fields to the UDIF file, consistent with the new ATTDFT/ICT output data, to indicate the test-point type of each accessible device pin, via, or pad. This new information is processed by the DORA2 software during its test-point selection process, which can add or modify selected test points as they are needed.

DORA2 Description. The DORA2[10,11] tool is a UNIX-based system that translates AT&T circuit-testing information from the design to the manufacturing process. DORA2 automatically translates circuit-connectivity data and simulation results into test programs, circuit-description files, and ICT fixturing layout files for many models of ATE.

DORA2 Enhancements. The DORA2 system was enhanced to align with the new process, taking advantage of the new information being supplied to the UDIF. Circuit description information input for DORA2 has come from the UDIF file since the mid-1980's. The UDIF file was created by the DORA project as a standard format to specify circuit-description information.

Test-Point Selection. The DORA2 test-point selection process analyzes all accessible points on a net to determine which point(s) should be selected to represent that net on the ATE test fixture. Currently, DORA2 does test-point selection for the following ATE: Teradyne L2XX and L3XX, Factron 333X, Hewlett Packard 3065 and HP3070, and GenRad 227X. However, with the new ATTDFT/ICT-derived test-point information in the FOCUS-created UDIF input file, the DORA2 test-point selection process will now be by-passed for those nets with ATTDFT/ICT-selected test points.

DORA2 users can override the ATTDFT/ICT-selected test points by supplying a user-control (constraints) input file. Various DORA2 output reports also have been updated to show the origination of the selected test points, ATTDFT/ICT or others.

Test Data File Updates. New software has been added to the DORA2 system to update the ATTDFT/ICT test-data file. The test-data file is the main output of the ATTDFT/ICT tools. It contains information about *all* accessible points in the circuit.

DORA2 customers are now requesting the UDIF and the test-data file from their suppliers, such as the layout group. Previously, only the UDIF was required. The DORA2 software will update this file so that its contents reflect the final selection of test points on the ATE test fixture. The updates to the ATTDFT/ICT-selected test points occur by means of the DORA2 algorithm, or new selections made by the test engineer.

Probe Style Utility. A new utility has been added to the DORA2 system to determine what type of probe is needed per selected test point. This software uses the new test-point diameter information that was added to the UDIF file by the FOCUS tool. With this information, and a user-supplied probe preference file, DORA2 can accurately pick the type (needle, star, crown, tri-needle, etc.) and size (100 mil, 75 mil, etc.) of a probe, per selected test point. With this probe information, the test engineer has a good estimate of how much it will cost to build a test fixture.

Summary

The evolution of structured testing has, until recently, followed at arms length the technology of the product tested. Significant strides in functionality at the device and CP level have led to large investments in test development and hardware. AT&T, however, has improved the quality of structured testing of its high-density SMT CP designs. Recent emphasis on such designs has created a definite need for new test techniques and design processes, especially at ICT, which is still the most economical and thorough assembly test in terms of development and equipment cost.

Incorporation of strong DFT practices during all phases of CP design, along with alternate techniques of test access, such as B-S (device and board internal), finer-pitch (closer spacing of) test probing, and new test-fixturing methods (external, physical access), serve to increase test coverage and decrease time-to-market. Structured-test access concerns are becoming an earlier part of design phases. Likewise, additional layout tool packages, such as ATTDFT/ICT and modifications of DORA2 to supplement test information transfer to the factories, are setting the stage for a more streamlined product design-to-test process. This applies especially to future, high-density SMT designs.

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