Non-Destructive Optical Techniques for Characterizing Semiconductor Materials and Devices

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In the information age, communications technology depends on the efficient manufacture of photonic and electronic devices. Optical testing promotes manufacturing efficiency by controlling the quality of incoming materials, providing rapid feedback for process improvements, and analyzing why a product has failed. New, non-destructive optical techniques are being used to measure key properties of semiconductor materials and devices. Optical mapping reveals defective regions in various types of wafers, as well as in semiconductor-based lasers and detectors used in AT&T's lightwave communication systems. New optical testing techniques include optical beam-induced reflectance (OBIR), whose signals are used to map silicon, and spatially resolved photoluminescence (SRPL), which performs high-resolution mapping of III-V semiconductor materials.

Introduction

To meet the demands of the information age, complex photonic and electronic products must be manufactured with high yield and low cost. Factories that manufacture such devices must rapidly transfer new designs from research to manufacturing, and create products that perform with high reliability in the field. Optical testing can help manufacturers attain these goals.

For decades, conventional optical microscopy has been used to inspect products. During "inspection," certain properties of a device are evaluated, but the product's functionality is not directly tested. Optical measurements of electronic device properties that directly relate to charge and voltage can test functionality with greater accuracy than can simple inspections. For photonic devices, optical techniques are often direct functional tests.

Testing costs, a major component in semiconductor manufacture, can be minimized by using non-destructive, rapid techniques to measure key parameters. Optical testing replaces more time-consuming, destructive tests by using non-destructive optical mapping to assess the quality of incoming semiconductor wafers. (During optical scanning, a laser spot moves across a 250×250 micron area. Mapping sweeps the small scanned area over a larger area, such as a wafer.) Optical mapping can also be used to evaluate the quality and uniformity of thin epitaxial layers grown on these wafers, providing rapid feedback to process engineers. Non-destructive testing early in the process also eliminates costs associated with the processing and subsequent device-level testing of defective material. When problems do occur, device-level tests and wafer-level maps can be compared to analyze reasons for failure.

This paper presents several examples of optical testing, describes two new optical techniques developed at AT&T, and reviews results in compound semiconductor and silicon-based processing. These examples include wafer-level maps of defect densities and/or polishing damage in bulk gallium arsenide (GaAs), epitaxial GaAs, bulk indium phosphide (InP), epitaxial indium gallium arsenide phosphide (InGaAsP), epitaxial silicon, and silicon-on-insulator (SOI) structures. Device-level scans in mounted semiconductor laser and detector structures revealed both process- and operation-induced defects. In each example, processing engineers were empowered to improve defective material — once testing methods uncovered when and where the defects existed.

Panel 1. Abbreviations, Acronyms, and Terms

APD — avalanche photodiode
CSBH — channeled-substrate buried heterostructure
DIC — differential interference contrast
ESD — electrostatic discharge
GaAs — gallium arsenide
InGaAsP — indium gallium arsenide phosphide
InP — indium phosphide
IR — infrared
LPE — liquid-phase epitaxy
MESFET — metal-semiconductor field-effect transistor
MOS — metal-oxide semiconductor
OBIR — optical beam-induced reflectance
PIN — p-type/intrinsic/n-type
PL — photoluminescence
RF — radio-frequency
SOI — silicon on insulator
SIMOX — separation by the implantation of oxygen
SRPL — spatially resolved photoluminescence
TEM — transmission electron microscopy

Electro-optical Testing Hardware

AT&T has developed two new optical systems to evaluate the spatial uniformity of semiconducting materials and devices. As Figure 1 shows, both systems photo-excite samples with a focused laser beam. The energy of this "pumping" beam, used to photo-excite samples, is higher than the bandgap of the semiconducting material under evaluation. As a result, absorbed photons generate electron-hole pairs near the conduction and valence band edges.

In compound semiconductors like GaAs and InP, a direct bandgap leads to radiative recombination of the electron-hole pairs. This radiative process, or photoluminescence (PL), is less efficient near defects that provide non-radiative recombination paths.[1] (A non-radiative recombination path is a pathway in energy that allows electrons to recombine with holes without emitting a photon. These pathways reduce carrier lifetime and, therefore, our signals.) The absence of non-radiative recombination paths leads to higher carrier lifetime and a stronger PL signal. Scanning the pumping beam across the sample produces a map of the defect density.

In elemental semiconductors like silicon and germanium, an indirect bandgap weakens the radiative recombination process at room temperature. Before non-radiative recombination occurs, however, the electron-hole pairs significantly alter the infrared optical properties of the sample. Specifically, they reduce the real part, and increase the imaginary part, of the refractive index.[2] As a result, the infrared reflectance is changed when a pumping beam is absorbed by the sample. The magnitude of this change is influenced by defects that reduce carrier lifetime. Again, scanning the pumping beam across the sample produces a map of the defect density.

Both systems detect signals whose intensity increases in proportion to carrier lifetime and, therefore, they approximate tests of device functionality. The spatial scans are used for wafer mapping and device testing. In wafer mapping, the scanned area is swept across a wafer while an image-processing system identifies and counts defects. This data can be used to generate color-coded maps of defect density. In device testing, the raster scan is positioned over critical portions of a device structure, as shown in Figure 2. The scans are spatially registered to the gate region of a metal-semiconductor field-effect transistor (MESFET), the absorbing region of a p-type/intrinsic/n-type (PIN) detector, and the active mesa of a semiconductor laser.

The SRPL System. The SRPL system uses a focused argon or near-infrared laser beam to pump the sample, while detecting broadband PL radiated from the surface. As the beam is scanned over a wafer, the SRPL system searches for changes in PL intensity, which indicate the presence of defects.[3]

The pumping beam is scanned in and out of the plane of Figure 1 by an acousto-optic deflector, and within the plane by a scanning mirror. The beam is then focused to a 1- to 2-micron scanning spot on the sample. A resolution element on the surface is exposed to a power density of 10^5 watts (W) per centimeter squared (cm^2) during a dwell time of about one microsecond. A field of 250×250 microns is scanned in roughly 33 milliseconds. Frame rates are compatible with video processing and video-cassette recorder (VCR) storage. Conventional spectral PL is usually measured at considerably lower excitation conditions. High-power density creates high signal-to-noise ratios, whereas the low dwell time

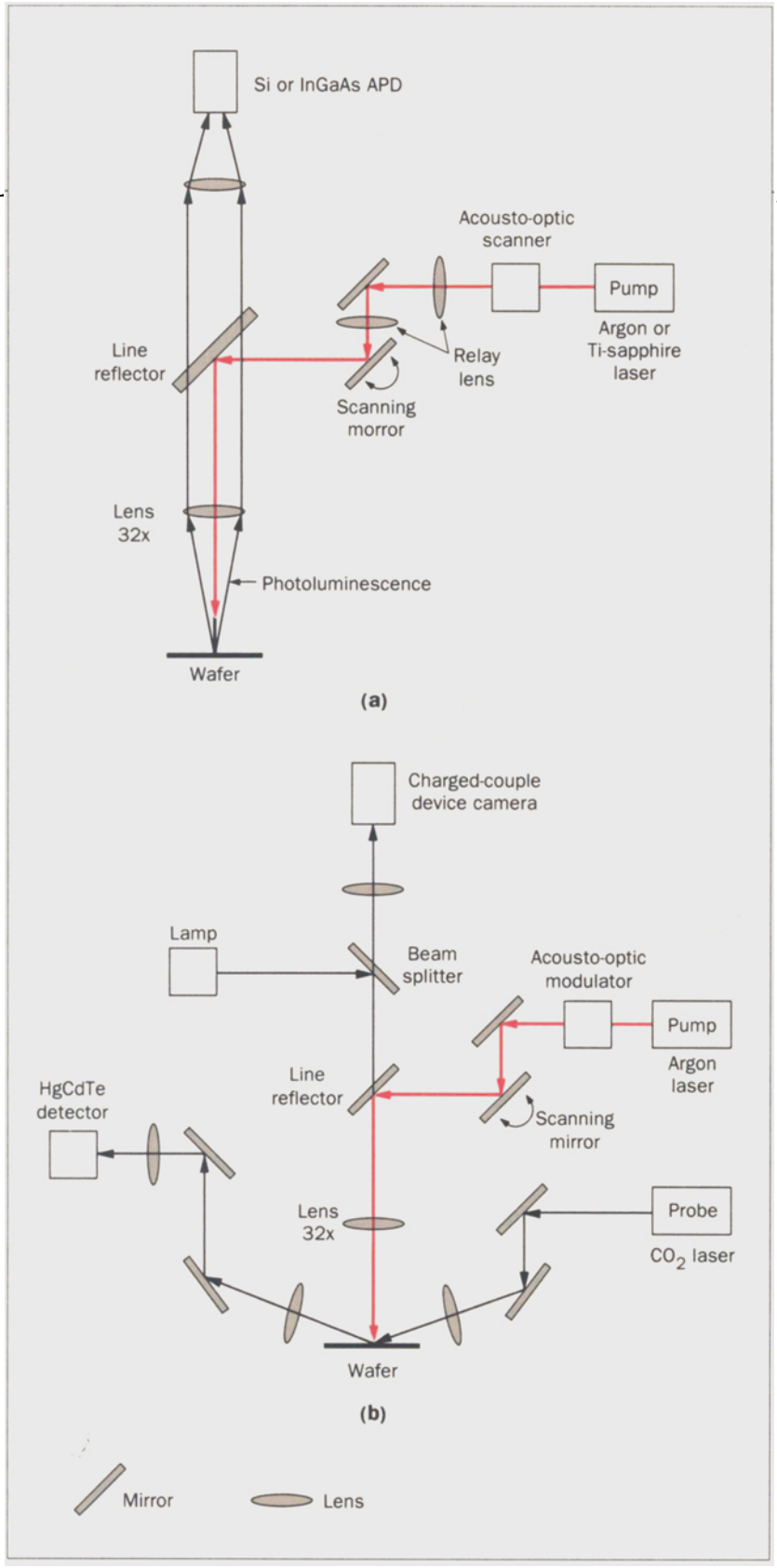

Figure 1. Schematics of the (a) SRPL and (b) OBIR spatial scanning systems. Both techniques scan a 1-micron spot within a 250 × 250 micron field of view.

associated with video scanning allows for non-destructive testing. Video frame rates also make wafer mapping possible in practical periods of time.

The PL beam is collected by the laser's focusing lens, passed through a dichroic beam splitter, and detected by an avalanche photodiode (APD). A silicon

APD detects PL emitted from InP, and an InGaAs APD detects PL emitted from InGaAsP. Additional filters reject the pumping beam and confine the PL spectral range to wavelengths emitted from critical layers within a device structure. A video processing board synchronizes the scanners, digitizes the signal, displays video frames, and analyzes the data. Localized defects (such as dislocations) are separated from elongated (polishing-related) defects using an image-processing algorithm developed for that purpose.

The OBIR System. The OBIR system pumps the sample with a focused argon laser beam, and then probes the resulting photo-induced change in the reflectance of a CO_2 laser beam. As the beams are scanned over a wafer, strong infrared (IR) modulation suggests that the material is defect free; weak IR modulation indicates electrically active defects.[4]

As Figure 1 shows, the pumping beam is chopped (i.e., turned on/off) at 30–50 kilohertz (kHz) by an acousto-optic modulator, reflected from a scanning mirror, and then focused to a 1-micron spot on the sample. About 5 milliwatts of power reach the sample, creating power density in the $10^5\,W/cm^2$ range — well below the damage threshold for silicon.

The CO_2 probing beam, directed towards the wafer near the Brewster angle, is detected by a mercury cadmium tellurium (HgCdTe) detector. About 1W of CO_2 radiation reaches the sample, creating a power density in the $10^2\,W/cm^2$ range. An amplifier locked to the frequency of the acousto-optic cell processes the signal from the HgCdTe detector. Processing only the portion of the reflected probing beam that becomes modulated at the chopping rate of the pumping beam produces a spatial resolution of 1 micron.

Scanning the pumping spot along the long axis of the elliptical probing spot, while moving a stage that supports the sample in the orthogonal direction, generates a scanned pattern on the sample. As the beams are scanned over the sample, an analog/digital board processes signals from the lock-in amplifier so they can be displayed on a video monitor. The 250×250 micron scan occurs in 30 seconds. OBIR scanning at video rates is under evaluation.

Even though the probe penetrates the sample, all photomodulation and, therefore, all detected defects are located near the surface, where the pump is absorbed. The penetration of the probe, however, can have an adverse effect on the signal. Scattering from the rough back surface of low-doped silicon imprints a disruptive speckle pattern on the display. Samples doped below about $7\times10^{17}/cm^3$ can be effectively scanned if the back surface of the wafer is polished. Standard metal-oxide semiconductor (MOS) wafers do not present this problem. Low-doped epitaxial films on high-doped wafers can exhibit occasional signal nulls resulting from destructive interference between reflections from the air/film and film/wafer interfaces.

Applications in Compound Semiconductors

The SRPL system maps III-V semiconductors, such as GaAs, InP, and their alloys. The next two sections describe results obtained using the SRPL system on wafers and in devices.

III-V Wafer Mapping. Wafers can be scanned after they are polished, and again after epitaxial deposition. SRPL scans in Czochralski, semi-insulating GaAs reveal a cellular network of dislocations.[5] These cells can assemble into so-called lineage boundaries, which are sheets of defective material extending along the growth axis of a crystal.[3]

Figure 3a shows a SRPL scan containing two discontinuous lineage boundaries and two continuous arcs of residual polishing damage. The wafer map shown in Figure 3b contains 5620 scans. A color-coded resolution element within the map represents the number of defects in a specific scan. Generated in about 15 minutes using near-real-time image processing, the map shows the four-fold symmetry typical of Czochralski GaAs.

Selective etching studies on experimental wafers delineate pits in the same sites that appear defective in the scans. Transmission electron microscopy (TEM) detects arsenic decoration in the dislocations, consistent with the fact that semi-insulating GaAs is As-rich.[3] The presence of high densities of decorated dislocations in a polished GaAs wafer influences the manufacture of MESFETs by allowing electrically active defects to reside within the ion-implanted channel region of a transistor.[6] These effects have been quantified by spatially registering the SRPL frame to a MESFET, as shown Figure 1. Defects within the gate region appear to reduce radio-frequency (RF) transconductance.[3] The impact of substrate defects can be reduced by forming devices in epitaxial GaAs layers deposited on the polished wafer. The SRPL system has also uncovered four-fold symmetry in

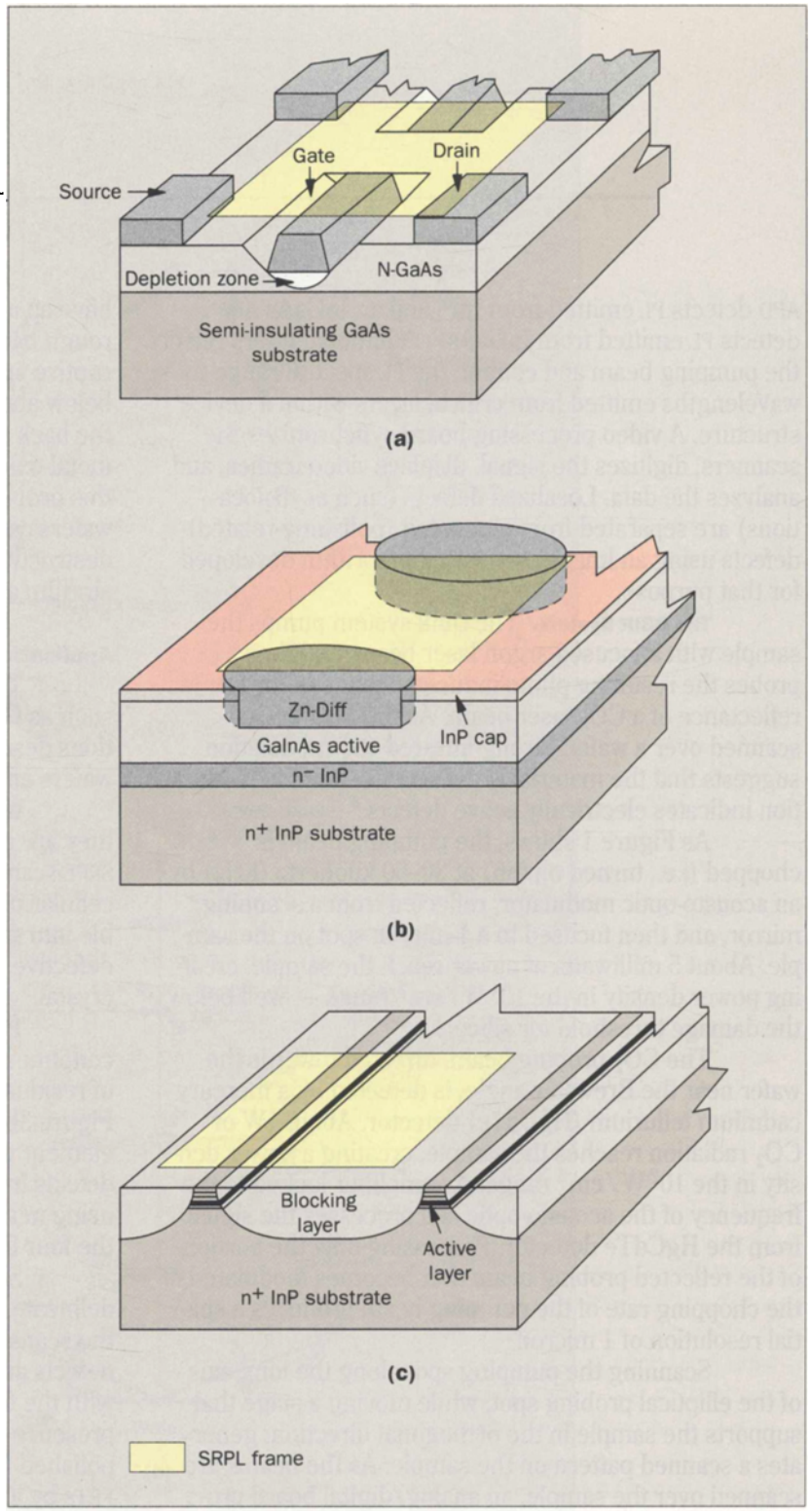

Figure 2. Examples of SRPL scanning in (a) MESFETs, (b) PIN detectors, and (c) semiconductor lasers. Micron-sized defects can be detected within the gate region of a MESFET, the absorbing region of a PIN detector, or the active mesa of a semiconductor laser.

the defect density of single layers of GaAs grown by molecular beam epitaxy, implying that defects in the starting wafer have threaded up through the epitaxial layer. Adding buffer layers can further reduce this threading process.

SRPL scans in bulk, iron-doped, semi-insulating InP detect localized regions of high-luminescent efficiency.[7] These bright spots have dimensions in the micron range, and a density approaching $1\times10^5/\text{cm}^2$. Selective etching and mass spectrometry of secondary ions have shown that these spots are dislocations containing excessive levels of silicon. These defects will probably generate parasitic capacitance that will adversely affect InP-based devices.

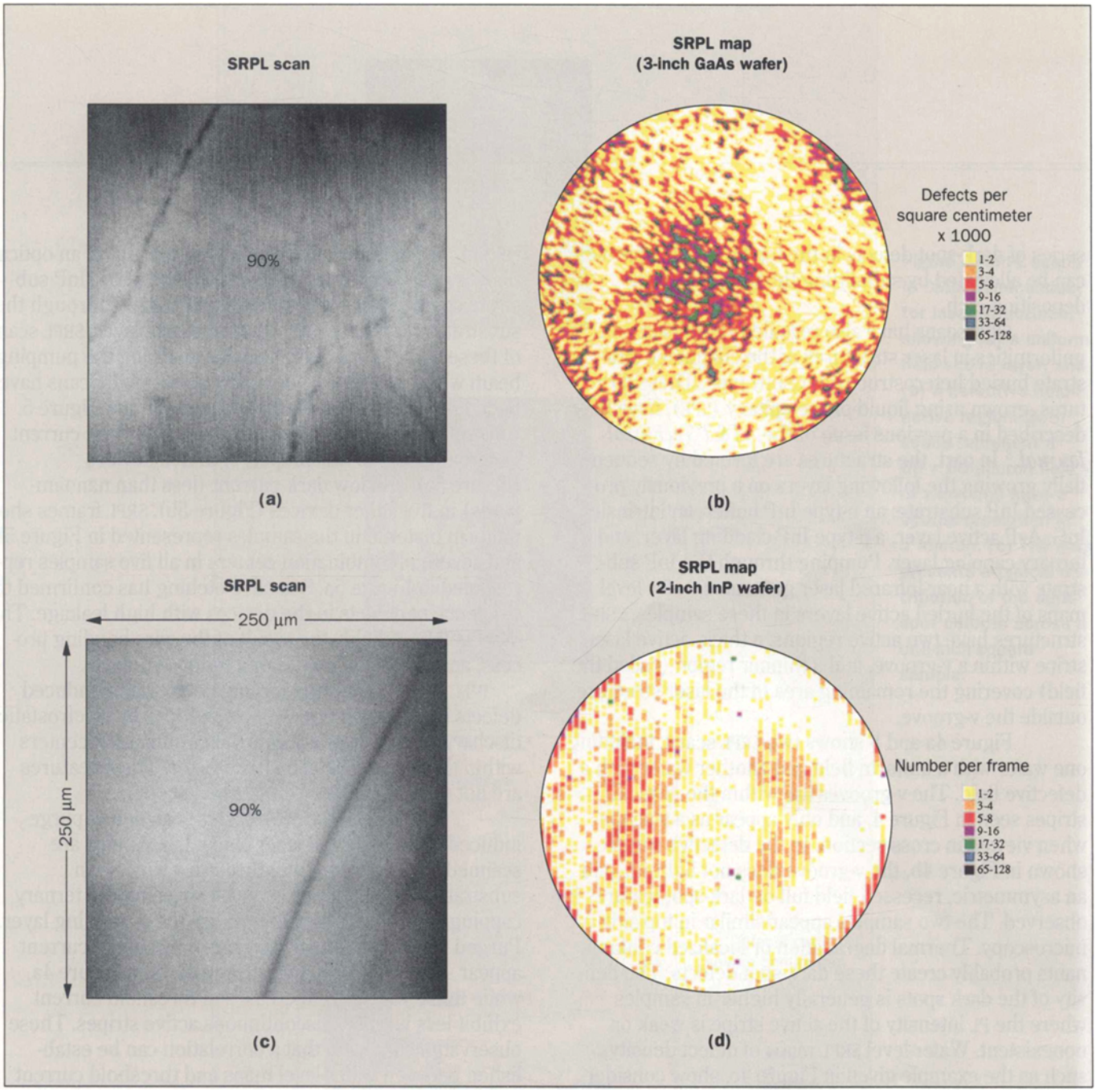

Figure 3. (a) A SRPL scan and (b) a map of a three-inch semi-insulating GaAs wafer. (c) A SRPL scan and (d) a map of a two-inch, zinc-doped InP wafer. Both scans represent a 250 × 250 micron field of view, and have a spatial resolution of 1 micron.

SRPL scans in bulk, sulfur- or zinc-doped semiconducting InP are used to evaluate polishing quality. Figure 3c shows a SRPL scan containing arcs of residual polishing damage in an InP wafer. This damage is not visible with conventional differential interference contrast (DIC) microscopy. The map in Figure 3d shows the spatial distribution of the damage, most of which results from the wafer-sawing process. Selective etching delineates morphology in the same sites that appear defective in the scans. Maps of similar wafers polished by different shops differ significantly. Some wafers exhibit virtually no polishing damage, while others are covered with a patchwork of scratch-like damage. As an experiment, a semiconductor laser structure was grown by vapor-phase epitaxy on a wafer with extensive polishing damage. After deposition, SRPL scans were taken by pumping the top (epitaxial) surface of the wafer, while detecting PL from the uppermost layer of the laser structure. These scans show that scratch-like features in the InP wafer grow up through the epitaxial layers, appearing as a

series of dark-spot defects in the top layer. This problem can be alleviated by submitting the wafers to a predeposition etch.

SRPL scans have also revealed significant nonuniformities in laser structures of the channeled substrate buried heterostructure (CSBH) type. These structures, grown using liquid-phase epitaxy (LPE), have been described in a previous issue of the *AT&T Technical Journal*.[8] In part, the structures are formed by sequentially growing the following layers on a previously processed InP substrate: an n-type InP buffer, an intrinsic InGaAsP active layer, a p-type InP-cladding layer, and a ternary capping layer. Pumping through the InP substrate with a near-infrared laser generates wafer-level maps of the buried active layers in these samples. CSBH structures have two active regions: a thick, active laser stripe within a v-groove, and a thinner region (called the field) covering the remaining area of the laser structure, outside the v-groove.

Figure 4a and b shows two SRPL scans, including one wafer with a uniform field and another wafer with a defective field. The v-grooves are within the vertical stripes seen in Figure 4, and only appear as a v-shape when viewed in cross-section. In the defective sample, shown in Figure 4b, the v-groove does not light up, and an asymmetric, recessed field full of dark-spot features is observed. The two samples appear similar in top-side DIC microscopy. Thermal degradation or localized contaminants probably create these dark-spot defects. The density of the dark spots is generally higher in samples where the PL intensity of the active stripe is weak or nonexistent. Wafer-level SRPL maps of defect density, such as the example given in Figure 4c, show considerable inter-wafer and intra-wafer variability. As the map demonstrates, it is difficult to determine the quality of a full wafer based on the destructive characterization of a piece from the edge of the wafer. In addition, the nondestructive nature of SRPL scanning allows mapped wafers to be processed into devices. As a result, wafer-level maps can be directly related to device-level tests.

Scans in Devices. The SRPL system can also scan discrete devices. As shown in Figure 2, scans in PIN detectors are spatially registered to the absorbing region of the device. These detectors, described in a previous edition of the *Journal*,[9] are processed by forming the following layers on an InP substrate: an n-type InP buffer, an intrinsic InGaAs absorber, and a p-type InGaAs region. In some packaged detectors, the end of an optical fiber is positioned near the back surface of the InP substrate so that light from the fiber propagates through the substrate and is absorbed by the InGaAs layer. SRPL scans of these devices are performed by inserting the pumping beam where the fiber is normally positioned. Scans have been taken on the ten devices represented in Figure 5. Current versus voltage plots indicate high dark current (microamperes to milliamperes) in five devices (Figure 5a), and low dark current (less than nanoamperes) in five other devices (Figure 5b). SRPL frames show uniform material in the samples represented in Figure 5b, and severe recombination centers in all five samples represented in Figure 5a. Selective etching has confirmed the existence of defects in the devices with high leakage. The defects are probably the result of the wire-bonding process, an example of processing-induced defects.

The SRPL system can locate operation-induced defects in PIN detectors. Defects induced by electrostatic discharge (ESD) appear as dark recombination centers within the active area of a PIN detector. These features are not visible in standard DIC microscopy.

In addition, the SRPL system can detect purge-induced effects in CSBH laser chips. Laser chips are scanned by either pumping through a window in substrate-side metallization, or by stripping the ternary capping layer and pumping through the p-cladding layer. Purged lasers with small changes in threshold current appear similar to the active stripe shown in Figure 4a, while those with large increases in threshold current exhibit less intense, discontinuous active stripes. These observations indicate that a correlation can be established between wafer-level maps and threshold current shifts during purge tests. SRPL may eventually provide rapid feedback to the growth systems. Further, SRPL maps can be used to reject heavily defective chips before manual pre-bond chip test, resulting in substantial savings in test time.

Applications in Silicon

The OBIR system maps group IV semiconductors, such as Si and Ge. The next two sections describe results obtained on MOS and SOI wafers.

Silicon Wafer Mapping. As the dimensions of MOS chips expand in response to increasing electronic functionality, the requirements for material quality become more stringent.[10] MOS IC processing generally is per-

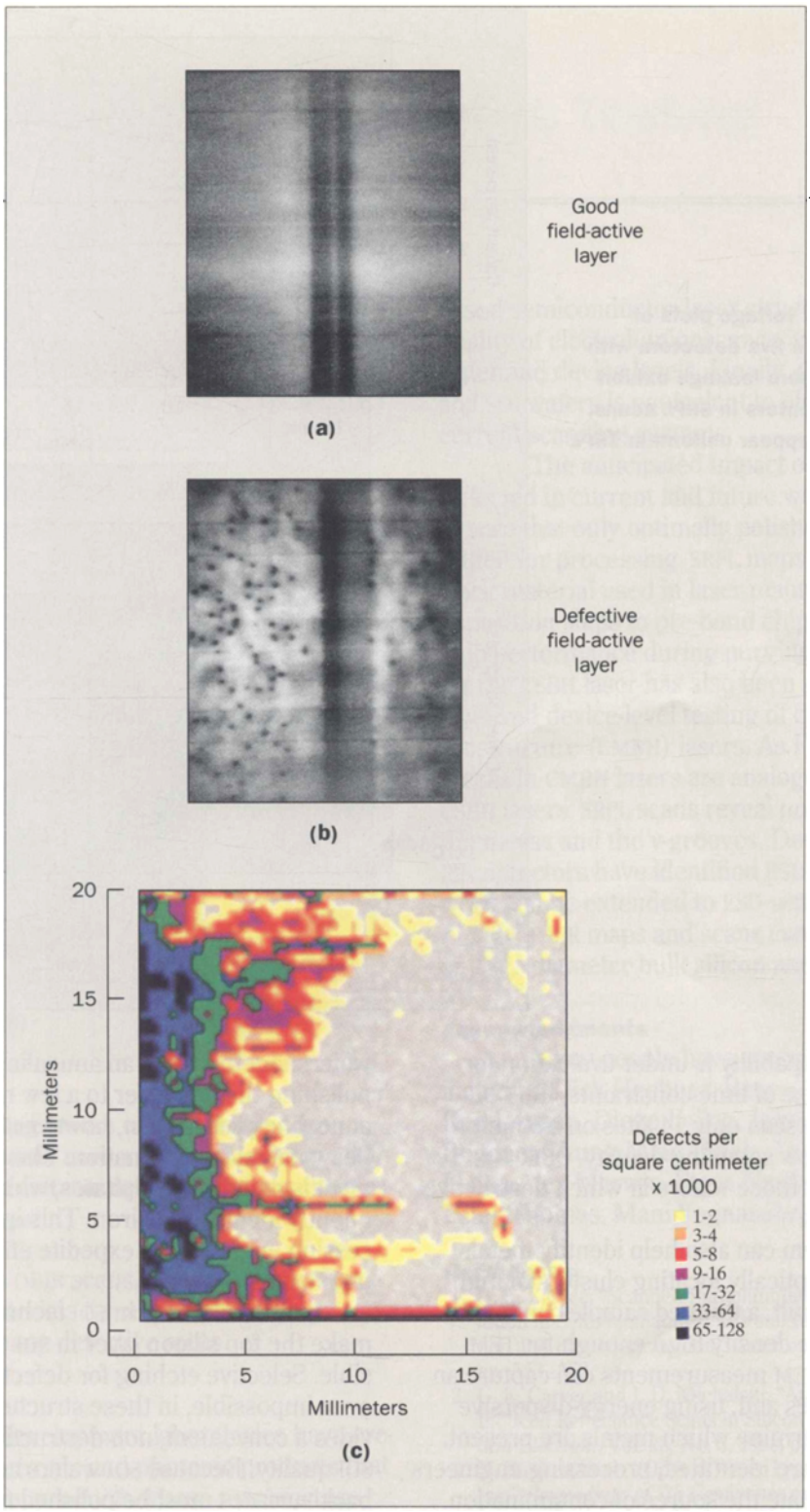

Figure 4. SRPL scans in CSBH semiconductor laser structures, showing (a) a uniform field-active layer, and (b) a defective field-active region. Both scans represent a 60 × 60 micron field of view, and have a spatial resolution of 1 micron. (c) The map presents a typical distribution of the dark-spot defects across a one-inch-square sample.

formed on highly doped silicon wafers (1×10^{18} Boron atoms per cm^3) coated with epitaxial silicon (1×10^{15} Boron atoms per cm^3). These p-/p+ wafers can become defective if metallic contamination is introduced during polishing or epitaxial growth processes. The OBIR system can detect micron-sized metallic precipitates, or *s-pits*, in these wafers.[4] If compared at the same locations on a wafer, OBIR scans and selective etching reveal the identical defect distribution. In production, selective etching is used to assess whether wafers contain defects. As the industry moves from 5-inch to 8-inch wafers and beyond,[10] the cost of each wafer will make destructive tests prohibitive. At 30 seconds per frame, the OBIR system requires several hours to map these large-diameter

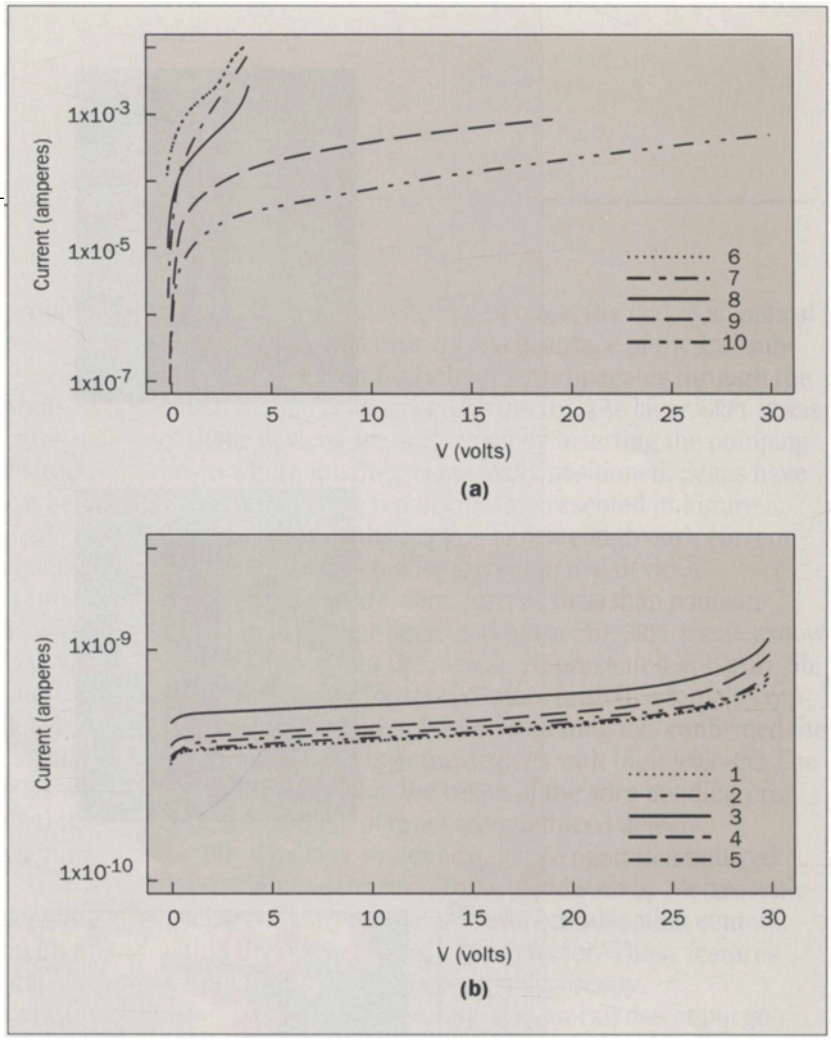

Figure 5. Current versus voltage plots of 10 PIN detectors. (a) The five detectors with microampere-to-milliampere leakage exhibit severe recombination centers in SRPL scans, while (b) the other five appear uniform in SRPL scans.

wafers. A video OBIR capability is under evaluation for this application. Because of time constraints, the OBIR system is often used to scan only 14 sites on a 5-inch wafer. Even with this low sampling density, OBIR identifies 40 percent of those wafers in which destructive etching reveals defects.

The OBIR system can also help identify metals within the defects by optically locating clusters of high-defect density. As a result, a thinned sample can be prepared with a precipitate density high enough for TEM analysis. Subsequent TEM measurements can capture an image of the precipitates and, using energy-dispersive x-ray analysis, can determine which metals are present. As soon as the metals are identified, processing engineers can pinpoint and eliminate the source of contamination.

Silicon-on-Insulator Mapping. High-voltage ICs are manufactured on dielectrically isolated silicon. OBIR has been successfully applied to two types of SOI structures: wafer-bonded SOI, and SOI formed by implantation. Figure 6 shows the basic building blocks of wafer-bonded SOI, along with an OBIR scan taken on an SOI wafer. Wafer-bonded SOI is formed by oxidizing a wafer, placing a second wafer on the oxidized surface, bonding the wafers together with an annealing process, and, finally, polishing the top wafer to a few microns thickness. The annealing process can, however, expose the SOI wafers to heavy metal contamination. The OBIR scan in Figure 6 reveals metallic precipitates, which TEM analysis subsequently identified as iron. This information allows processing engineers to expedite efforts to remove the contamination.

Researchers in SOI technology are striving to make the top silicon layer in SOI structures as thin as possible. Selective etching for defect delineation is difficult, or even impossible, in these structures. OBIR scanning provides a convenient, non-destructive method for assessing SOI quality. Because SOI wafers are not heavily doped, the back surfaces must be polished for OBIR scanning.

Implanted SOI is called SIMOX (separation by the implantation of oxygen).[11] SIMOX-based SOI is formed by implanting oxygen into silicon wafers, and then performing an annealing process. After the anneal, SIMOX still contains high densities of dislocations. OBIR scans in SIMOX reveal few defects, implying that the dislocations are not electrically active. Exposure of clean SIMOX to a source of metallic contamination can activate the defects,

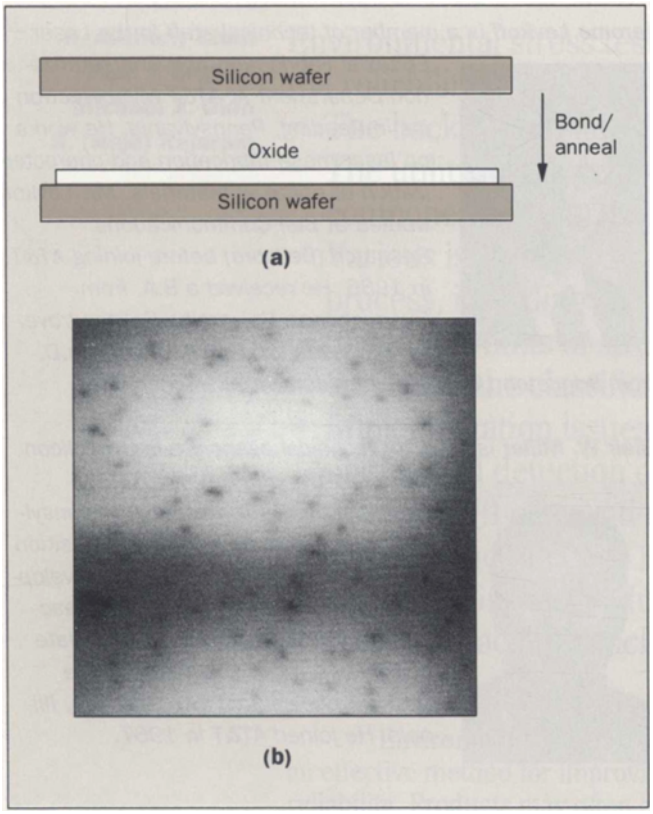

Figure 6. (a) Basic building blocks of wafer-bonded SOI materials. (b) This OBIR scan covers a 60 × 60 micron field, and reveals micron-sized metallic defects, later identified as iron, in the top silicon layer.

making them visible in OBIR scans. Thus, OBIR can track the quality of these materials through a processing sequence, and identify any defective steps.

Conclusions

Research and development laboratories have created a vast array of electronic and photonic products that fuel the information age, products whose manufacture can be made more efficient by using optical testing. Optical testing can improve both the quality control of incoming wafers and the epitaxial processes that produce device structures, and help to analyze device failures. The SRPL system and the OBIR system address these goals in a non-contact, non-destructive manner. SRPL scanning in GaAs exhibits spatial resolution and contrast that rivals cathodoluminescence. SRPL scanning in InP-based semiconductor laser structures matches the image quality of electroluminescence, yet functions at both the wafer and device levels. Finally, OBIR scanning in silicon and SOI wafers is equivalent to electron-beam-induced current scanning systems.

The anticipated impact of these techniques is reflected in current and future work. SRPL maps can ensure that only optimally polished InP wafers are submitted for processing. SRPL maps and scans can also track material used in laser manufacture, from epitaxial deposition steps to pre-bond chip testing, and, finally, to chip performance during purging. Work reported here for the CSBH laser has also been applied to both wafer-level and device-level testing of capped mesa-buried heterostructure (CMBH) lasers. As Figure 2c shows, the mesas in CMBH lasers are analogous to the v-grooves in CSBH lasers. SRPL scans reveal non-uniformities in both the mesas and the v-grooves. Device-level SRPL scans in PIN detectors have identified ESD-induced damage. This work can be extended to ESD-sensitive APD structures. Finally, OBIR maps and scans can help ensure the quality of large-diameter bulk silicon and SOI wafers.

Acknowledgments

Many people have contributed to this work, including Dick Heebner, Renee Moore, Vince Zaleckas, Ken Benson, Diego Feijoo, John Florio, Karen Grim-Bogdan, Chung-Ming Hsieh, Andreas Leiberich, Chuck Lentz, Alex Merwin, Steve Napholtz, Alex Robertson, Peter Thomas, Mani Yegnasubramanian, and Dan Yoo.

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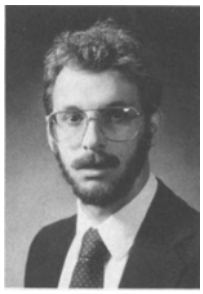
(Manuscript approved February 1994)



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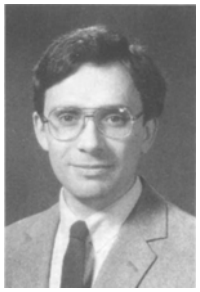

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