# Dielectric Materials for Advanced VLSI and ULSI Technologies

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Advancements in very-large-scale integration (VLSI) and ultra-large-scale integration (ULSI) of semiconductor devices result in complex, multilevel interconnect schemes and increased dependence on dielectric materials. These material systems (how the various materials in an integrated circuit [IC] are united together) are used in a variety of thin-film applications, such as insulators, ion implanting, and pattern-etch masking, as well as in final device passivation. For such applications, thin films must exhibit good mechanical, chemical, and electrical properties that are compatible with IC processing schemes. Thin films must also meet ease-of-manufacturing requirements. These stringent demands require a clear understanding of the material systems used in advanced technologies. Therefore, dielectric materials are selected according to applications, deposition process and hardware, film properties, and device integration. Thin-film deposition techniques, including plasma-enhanced, low-pressure thermal, electron-cyclotron-resonance chemical vapor, and spin-on are presented. Emerging deposition processes and new dielectrics are also discussed.

## Introduction

Silicon (Si) technology has remained the dominant force in IC fabrication, and is likely to retain this preferred position (over gallium arsinide and germanium) for the foreseeable future. The number of devices manufactured on an IC chip typically exceeded one million in the early VLSI era, with minimum line sizes approaching submicron (<1.0 μm or <0.04 mils) geometries. Advanced VLSI and ULSI technologies represent a one-to-two-orders-of-magnitude increase in active elements, with line sizes in the sub-one-half-micron regime (<0.5 μm or <0.02 mils).

The design of ICs is functionality application-oriented; that is, the details of IC design are strongly dependent on the intended use or application of the device. Typical IC applications include digital logic circuits, dynamic and static memory boards, microprocessor devices, and signal-processing equipment. A composite drawing of the circuit, an IC design layout, is divided into processing levels—gate electrodes on one level, contact windows from interconnect metal routing to device functions on another, and so forth. The steps used to define geometrical features are referred to as *mask levels*. The proposed design layout then undergoes a series of computer-simulated functionality tests. Interactive graphic displays and digitizers convert the geometrical layout to digital data that are used to drive a computer-controlled, electron-beam, pattern-generation machine. The electron-beam machine can transfer the pattern directly to the Si substrate. More frequently, however, the machine is used to transfer the pattern onto chrome patterns on glass substrates, called *masks* or *reticles*. The IC is made by sequentially transferring the features from each reticle—level by level—to the Si substrate. The patterns are transferred first into a photosensitive polymer material, also known as *photo resist*, which is then used as an etch mask for reactive-ion-etch (RIE) transfer into the polysilicon, dielectric, or metal materials. For

**Panel 1. Abbreviations, Acronyms, and Terms**

Al—aluminum

APCVD—atmospheric-pressure chemical-vapor deposition

BHF—ammonium-fluoride/hydrogen-fluoride buffer or mixture

BPSG—boron-doped and phosphorus-doped silicon glass

CD—critical dimension

CMOS—complementary metal-oxide semiconductor

CMP—chemical-mechanical polishing

CVD—chemical-vapor deposition

dielectric—a material that does not conduct electricity

DCS—dichlorosilane

DRAM—dynamic random-access memory

electron-cyclotron-resonance microwave discharge—an emerging film-deposition technique

ECRCVD—electron-cyclotron-resonance chemical-vapor deposition

EPROM—erasable programmable read-only memory

FOX—field oxide, an element of an active device on an IC

glow discharge—plasma created by the action of magnetic and electric fields on gaseous materials

$g_m$—transconductance gain

GPa—gigapascal

hygroscopic—readily absorbing moisture

IMD—intermetal dielectric

LDD—lightly doped drain

LOCOS—local oxidation of silicon

LPCVD—low-pressure chemical-vapor deposition

"marathon run"—an extended period of product production that is monitored by passive data collection for critical attributes about a dielectric film

mask—a glass plate having a chrome overlay, which accepts an IC's circuit layout as generated by an electron-beam pattern-generation machine

mask levels—the steps used to define an IC's geometrical features

MOCVD—metal-organic chemical-vapor deposition

MOS—metal-oxide semiconductor

MPa—megapascal

nm—nanometer ($10^{-9}$ m)

OMCTS—a chemical, octamethylcylotetrasiloxane

PBL—poly-buffered local oxidation of silicon

PECVD—plasma-enhanced, chemical-vapor deposition

photo resist—a photosensitive polymer material used in the manufacture of ICs

planar—flat or level surface, often used to describe a dielectric film

polyimide—a polymeric organic material used as protective top coats in IC fabrication

PVD—physical vapor deposition

reticle—a synonym for "mask"

RC—a measure of time in the IC manufacturing process (a characteristic response time of an IC)

reflow—term used to describe a flowable material with a contact window cut

RF—radio frequency

RIE—reactive ion etch, a process by which an IC's circuitry is transferred to a polysilicon, dielectric, or metal substrate

RTACVD—rapid-thermal-anneal chemical-vapor deposition

SALICIDE—self-aligned silicide, a process used to align IC dielectric films

Si—silicon

SOG—spin-on glass, a dielectric-film deposition technique

SRAM—static random-access memory

step-coverage—as-deposited dielectric-film conformality

stoichiometry—the relationship between the components of a chemical compound

TEOS—a chemical, tetraethoxysilane

TOMCATS—a chemical, 2,4,6,8-tetramethlcyclotetrasiloxane

ULSI—ultra-large-scale integration

UV—ultraviolet, a category of visible light

VCR—vacuum-compressed ring

VLSI—very-large-scale integration

$V_t$—threshold voltage

example, an ion-implant, drive-in, oxidation, metalization, or deposition operation may take place between each successive image-transfer process.

Increasing semiconductor device integration by feature size reduction results in increased levels of interconnect and increased dependence on—and utilization of—dielectric and insulating materials (films) in advanced VLSI and ULSI. These films are used in many applications, including insulation, diffusion, implantation, etch masking, and final passivation of IC chips.

For such applications, these films must meet the following specifications:

- High quality and freedom from defects;
- Excellent uniformity of wafer and batch thicknesses, dopant coating, and material properties;
- Inherently planar or easily planarized;
- Conformance with thermal budget;
- High mechanical strength;
- Low and controllable mechanical stress;
- Low dielectric constants;
- Moisture resistance;
- Effective resistance to alkali metals;
- Superior adherence to the underlying layers; and
- Chemical, radiation, photoactive, and thermal stability.

These stringent specifications require a clear understanding of the dielectric and insulating materials used in the technologies, deposition processes, and hardware. The materials, material-deposition chemistry, physical properties, and device applications of dielectric and insulating films are presented in this paper. Films deposited by plasma-enhanced, chemical-vapor deposition (PECVD), low-pressure chemical-vapor deposition (LPCVD), and spin-cast methods (spin-on glass [SOG] and polyimide), are discussed. References are also made to emerging dielectrics—for example, tantalum oxide ($Ta_2O_5$), and film-deposition techniques, such as electron-cyclotron-resonance microwave discharge.

This paper consists of four sections: applications; deposition-process considerations; film-deposition hardware; and dielectrics in advanced VLSI and ULSI.

## Applications

Fabrication of modern VLSI and ULSI circuits depends heavily on dielectric films. These films provide electrical insulation between metals and protection from the environment. In some special cases, dielectric films are also used as sacrificial layers in the integration process. There are three major advantages of using deposited films:

- No limitation on substrate material,
- No substrate consumption, and
- Low deposition temperature with high deposition rate for throughput.

Application details for these deposited dielectric films are illustrated schematically in Figure 1[1] by a submicron, four-level interconnect, twin-tub, complementary metal-oxide semiconductor (CMOS) cross section.

IC fabrication involves several layers of pho-tolithography and dry-etch patterning to define active-device circuit areas. Patterning is followed by additional layers of interconnect routing to connect the device elements for a particular functional application. The CMOS structure of Figure 1 is built on a P+<100> Si substrate, with ion-implanted N+ and P+ tub areas. The field oxide (FOX), polysilicon, and ion-implanted source/drain areas represent elements of the active devices. The lightly doped drain (LDD) spacer is a deposited dielectric material, which serves as a partial ion-implant mask. The LDD spacer also enhances the smoothing profile of the dielectric, one layer over the topography of active areas.

The first dielectric (D1) layer isolates the first metal (M1) interconnect routing from the active circuit areas. Windows are etched through the dielectric and are typically filled with a metal plug material, such as tungsten, to make contact between active circuit elements and the metal routing. The metal routing typically incorporates a stack consisting of aluminum (Al) alloy cladded with barrier materials, such as titanium (Ti) and titanium nitrate (TiN). In general, the metal materials are deposited by physical vapor deposition (PVD) methods. Dielectric layers, depicted as basically homogenous, may consist of multiple layers as the particular application would require. This is discussed later in further detail.

The first major step in the device-fabrication integrated process is to deposit and pattern a silicon-nitride ($Si_3N_4$) film (an oxygen-and-water diffusion barrier) for FOX formation, which is thermally grown and is the fundamental isolation for all devices throughout the entire IC chip. This diffusion-mask dielectric is normally removed after FOX formation.

Some of the problems encountered by process engineers in patterning the gate, such as critical-dimension (CD) control for a gate length of <0.5 μm, have led to the use of dielectrics as etching masks (hard masks). During the gate-etch process, the traditional organic photo-resist mask can lead to line-width growth due to photo-resist redeposition. Furthermore, the organics tend to cause loading effects in an RIE discharge, leading to pattern dependence on density. As a solution, dielectric films (either silicon dioxide [$SiO_2$] or $Si_3N_4$) are used for gate-etch masks. Choice of hard-mask material (either oxide or nitride) depends on the gate material (Si or silicide). Removing or not removing the hard mask after processing depends on process complexity. The hard mask may remain on the gate as an implant or diffusion mask for source/drain doping.
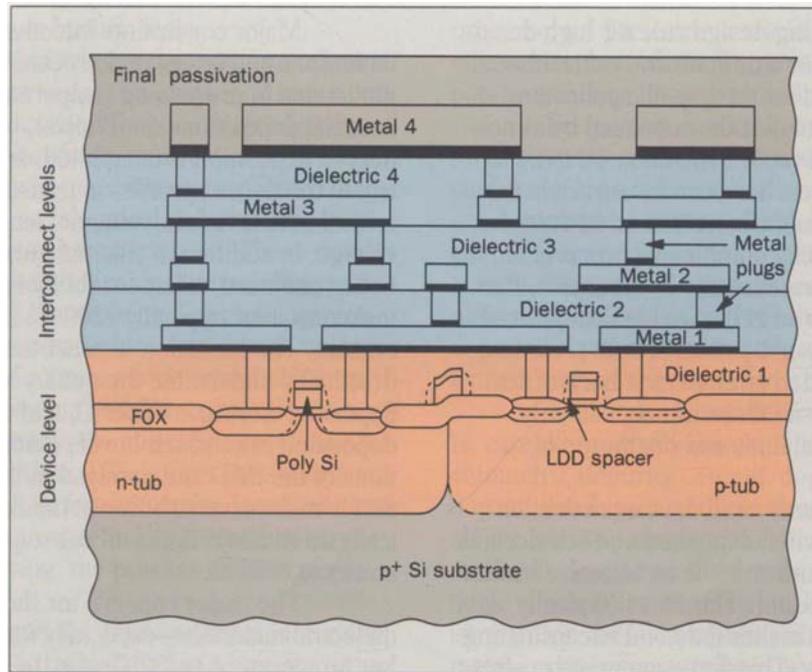
Figure 1. This illustration depicts application details for deposited dielectric films as applied to VLSI and ULSI circuits. The schematic cross section shows a submicron, four-level interconnect, twin-tub CMOS device.

Dielectric materials, including tetraethoxysilane (TEOS), are also used as spacers for preventing short circuits from source/drain to gate, and also as ion-implantation masks for LDDs. Spacers are critical, especially in the production of advanced metal-oxide semiconductor (MOS) devices using the self-aligned silicide (SALICIDE) processes.

The dielectric film that insulates a transistor from metalization is generally referred to either as D1 or as the interlevel dielectric. This film performs several key functions, such as providing a sodium barrier and topography smoothing. The film normally consists of two parts: undoped and doped oxides. Undoped film acts as a diffusion barrier for the impurities in the doped film. The dopants are phosphorus (P) and boron (B). P-dopant typically serves as the sodium gettering or barrier. Sodium and other mobile ions are known as fatal contaminants to a MOS device, because they will shift the threshold voltage of both active and parasitic transistors. However, the as-deposited P-doped oxide forms overhangs or protruding side walls that cover the gate, making subsequent deposition difficult.

The *step-coverage*, or conformality of oxide can be improved by high-temperature treatment following film deposition, which softens and "flows" the oxide. Flow temperature can be drastically lowered with the addition of dopants, such as B, germanium (Ge), or arsenic (As). The choice of dopant concentrations in BP-doped Si glass (BPSG) is a complex process-integration issue. High dopant concentration can lower the thermal budget while improving smoothness. Too much phosphorus may corrode Al, and too much boron makes the oxide film hygroscopic. Furthermore, high dopant concentrations render the films unstable and susceptible to crystallite ($BPO_4$, $P_2O_5$) formation.

The dielectric film between metal layers is generally referred to as intermetal dielectric (IMD), or simply dielectric 2, 3 (D2, D3), and so forth. The importance of dielectric applications for IMD has increased significantly due to the development of multilevel-interconnect technology. As Si devices shrink in size and circuits become more complex, multilevel-interconnect technology for chip-size reduction—as well as speed and performance—will improve.

PECVD of oxide is widely used in Si devices. In multilevel-interconnect technology, higher-level process temperatures are limited by the presence of first-level metal (typically an Al alloy). Therefore, low-temperature PECVD processes (<450°C), which use plasma rather than thermal energy to promote chemical reactions, are inherently appealing. As the aspect ratio (defined as the feature-height to feature-spacing ratio) of metal lines

increases with the shrinking-design rule for high-density circuits, gap fill becomes a difficult and critical issue. SOG has been widely used for the gap-fill application.

Recently, ozone ($O_3$)-TEOS, deposited by atmospheric-pressure chemical-vapor deposition (APCVD) at low substrate temperatures, has become attractive for the same gap-fill application. Use of SOG or O3-TEOS for gap fill increases processing complexity, however, because both materials are basically hygroscopic. For device application, a layer of PECVD oxide is deposited first, before applying SOG or $O_3$-TEOS. A PECVD oxide-capping layer is also needed after an etch-back of SOG or $O_3$-TEOS, such that gap-fill materials remain only in trenches between metal lines and not on top of metal lines.

The most commonly used device-passivation layer for advanced VLSI, when deposited on Si devices, is PECVD ($Si_3N_4$), which is known to be an effective barrier against both water and sodium. Hardness (typically >20 GPa) of this material also makes it a good encapsulating layer for scratch resistance. This film's compressive stress generates metal-reliability issues, however, and prompts process engineers to use a buffer layer of PECVD oxide between nitride-cap and metal lines. PECVD oxynitride (SiON), which has properties between those of nitride and oxide, is also a popular choice for this application.

Several important dielectric materials and processes are specific to memory-device applications. For example, in dynamic random-access memory (DRAM) applications, the dielectric film for charge storage is one of the most crucial materials in device fabrication. Although $SiO_2$ is the most widely used charge-storage material, new high-dielectric-constant materials, such as $Ta_2O_5$, are needed for use in high-density storage-devices. Chemical-vapor-deposition (CVD) oxide is also widely used in memory devices for other purposes, such as placement between polysilicon layers, for both static random-access memory (SRAM) and erasable programmable read-only memory (EPROM) chips. The CVD process produces highly conformal films, which make this technique the one most favored for dielectric film applications.

**Requirements.** The primary requirements for these dielectric films are:
- Reliability and quality of device performance,
- Ease of manufacturing, and
- Cost efficiency.

Major constraints include process-temperature limitations and integrated-process compatibility. The limitations in processing temperature for dielectric-material depositions (and flows), before metal-interconnect Al deposition is completed, are mainly due to control of the dopant profiles in transistors. Profiles are critical in determining channel length and threshold voltage. In addition, if silicides (for example, $TiSi_2$ and $CoSi_2$) are used, silicide stability imposes a severe thermal constraint (typically $\leq 800°C$) for subsequent processing. The limitation in processing temperature can drastically undermine the quality and properties of the deposited dielectric material, and can also reduce the deposition rate, which lowers throughput. For applications of the IMD and passivation layer, process limitation is more severe, because the first level of metal (typically an Al alloy) limits all subsequent process temperatures to <450°C.

The major concern for the quality of these dielectric materials—especially for those deposited at low temperature (<450°C)—is the effects of transistor degradation and long-term device reliability. Low-temperature-deposited dielectric materials tend to contain impurities and byproducts (intermediates) from the source materials, such as carbon, water, silanol (Si-OH), and Si-H. Some materials, such as $O_3$-TEOS and SOG, tend to be hygroscopic, which is an even greater concern. Atomic H, water, and silanol are known to accelerate the hot-electron effect, shift threshold voltage $(V_t)$, and degrade transconductance gain $(g_m)$. Compressive or tensile stress, which should be <100 MPa, is also a critical property of dielectric films. Serious metal-reliability issues, including electromigration and stress-induced voiding, are linked to high compressive stress (>100 MPa) and the hardness of the dielectric films, while film cracking is attributed to high tensile stress.

Film morphology and gap-fill capability are also important issues. For example, a conformal and smooth D1 is important to metal yield. Good flow of D1 is essential. Otherwise, extra steps for smoothing the profile are required. For IMD applications, good step-coverage without voids between metal lines is crucial. Voids not only create cosmetic problems, but also introduce process complications and metal-reliability issues. Device or chip yields can suffer significantly if these requirements are not met. Yield issues can be readily

detected during aging or burn-in tests.

Ease of manufacturing is the most important requirement after process development. The major concerns about ease of manufacturing are defect density, uniformity, process robustness, and cost of ownership. Defects and uniformity issues can be complicated, and they result from process (chemical and physical) reactions, or from the reactor hardware used. These defects and uniformity issues are critical in determining yield (good chips per wafer). As evolving Si technology continues to shrink device dimensions (<0.50 μm), enlarge chip size (>2 cm²), and increase wafer size (>200 mm), defect-density requirements and film uniformity become more important. Currently, the sub-0.5-μm objective for defect density is fewer then 0.03 defects per square centimeter (defects >0.2 μm); for uniformity, less than three percent (3σ) for 200-mm wafers. For the technology to succeed in manufacturing, the process window needs to be solid or robust.

Cost efficiency is the final requirement for any process or equipment to be installed in a manufacturing plant. The main parameters in calculating cost of ownership are throughput (wafers per hour), capital expenditures required for hardware and space, material costs, and maintenance schedules.

## Deposition-Process Considerations

This section discusses the essential attributes of current dielectric-film deposition processes and the materials used in VLSI and ULSI technologies. The materials are $Si_3N_4$, undoped and doped silicon oxides, SOG, polymers (polyimides)—and emerging dielectrics, such as $Ta_2O_5$. These films are used in a variety of applications: insulation, diffusion, implantation, mask etching, and final device passivation.

VLSI and ULSI dielectrics must exhibit good mechanical, chemical, and electrical properties. They must be reproducible: the physical and chemical properties of the dielectric materials must repeat from deposition to deposition, reactor to reactor, and location to location. The dielectric films must also be stable—chemically, photoactively, and thermally—as well as when exposed to high-energy radiation.

With increased complexity of interconnect levels, thermal constraints have become an important concern. These constraints have necessitated film depositions at low temperatures and the use of more volatile

precursors. [2] Dielectric materials are invariably deposited as amorphous films, because their crystallization temperatures are very close to their melting points.

For certain applications, where high temperatures associated with APCVD and LPCVD are undesirable, such as in Al-based metalization schemes, dielectric films are deposited by PECVD, electron-cyclotron-resonance chemical-vapor deposition (ECRCVD), atmospheric pressure $O_3$-TEOS, or by liquid-dispense and spin-on techniques. The electrical and mechanical properties of films deposited by these techniques are easily controlled over a much larger range than films deposited by LPCVD.

The attributes of dielectric-film quality that must be carefully controlled include layer thickness, stoichiometry, impurity content, dopant concentration, dopant distribution, pinhole density, adhesion, conformal ability, intrinsic stress, and dielectric properties. These attributes depend on the details of film-deposition conditions, which determine the local molecular-level chemistry within these amorphous films. For example, alkali metal-ion contaminants have been reported to break up film structure and degrade the physical properties of $SiO_2$ film.[3,4]

As-deposited, dielectric-film conformal ability becomes a critical issue when dealing with the small geometries and very high aspect ratios associated with advanced VLSI and ULSI technologies. For example, interlevel dielectric films cannot be planarized by high-temperature reflow in an Al-alloy-based scheme; hence, the films must be very conformal. This constraint—and the need for improved process safety—have resulted in a trend toward the use of liquid organic precursors for dielectric films.

As-deposited film step-coverage is a strong function closely associated with process conditions, reaction chemistry, and kinetics. Choice of precursor influences step-coverage. For example, organic precursors are known for their improved oxide conformal ability, compared to hydride precursors, such as silane ($SiH_4$). Also, deposition pressure influences the mean free path of reactive species, thus influencing step-coverage. At high temperatures, the effects of surface mobility, sticking coefficient, and reaction kinetics converge to produce high step-coverage. Highly conformal films can also be produced from organosilicon-ozone (for example, TEOS-$O_3$) processes at atmospheric and subatmospheric pressures for profile filling. On the other hand, spin-coated

processes result in planar-fill profiles.

Reflectivity of dielectric films affects pattern resolution and definition by optical lithography. Reflectivity of UV-visible light (for example, 420 nm and 365 nm) depends on film thickness and density, which are attributed to dispersion-distortion effects.

**Silicon Nitride.** An effective barrier against moisture and alkali-metal contamination, this material is also used as an oxide etch mask, and has excellent dielectric properties. Depending on the application, $Si_3N_4$ films are deposited by a variety of CVD techniques and precursors.

$Si_3N_4$ can be deposited by using a variety of chemistries, such as those listed in Table I.[3-7] Silylimide ($Si[NH]_2$), and possibly its polymers, are the principal precursors to $Si_3N_4$. These materials appear to form spontaneously when mixing the reactants in a hot reactor. Or, they may be produced by free radicals in PECVD reactors. In PECVD, hydrogen is incorporated into the nitride films as N-H, and Si-H functional groups and films are represented as $Si_3N_4H_x$.

From thermal-budget and throughput considerations, $SiH_2Cl_2$ (dichlorosilane, or DCS) is currently the preferred Si precursor for $Si_3N_4$ films. However, the deposition process using this gas is plagued with high defect densities due to the formation of white, powdery $NH_4Cl$ by-products. This apparent limitation can be overcome by combining hardware and process modifications.

The stoichiometry of the deposited film depends on the $NH_3$-to-Si precursor ratio, as well as deposition conditions. Stoichiometry determines the film's properties, such as refractive index, etch rate, color, water permeability, thermal stability, and intrinsic stress. The refractive index of $Si_3N_4$ films is a bonding-density-weighted, linear combination of the refractive indices of stoichiometric $Si_3N_4$ and Si, respectively.

LPCVD $Si_3N_4$ films tend to be Si rich when the ratio of Si to nitrogen precursors is high. On the other hand, nitrogen-rich films do not form—irrespective of the relative concentration of the nitrogen precursor. Low-temperature $Si_3N_4$ films (PECVD and ECRCVD) are generally hydrogenated, nonstoichiometric, and can be deposited over a wide range of stoichiometries. Si-rich films exhibit higher refractive indices, and higher etch rates in hydrofluoric acid, than stoichiometric films. These differences in physical and chemical properties may be attributed to the existence of trivalent Si (dangling bond) centers in the bulk of Si-rich films.

Mechanically, LPCVD $Si_3N_4$ films tend to crack and dislocate at the edges during oxidation. This is due to the enormous intrinsic stress caused by differences in the thermal expansion coefficients between $Si_3N_4$ and the Si substrate. Hydrogenated nitride films deposited by PECVD are less stressed.

The use of $Si_3N_4$ films in masking applications, such as local oxidation of Si (LOCOS) and poly-buffered local oxidation of Si (PBL) isolation, is based on their slow rate of oxidation. Nevertheless, $Si_3N_4$ films do oxidize at temperatures >900°C in the presence of oxidants, such as water or oxygen. Conversion of $Si_3N_4$ to $SiO_2$ is a chemically facile reaction ($\Delta G$ = -276 kJ/mole), but one which is apparently limited by the diffusion of the oxidant through the nitride film. Furthermore, oxidation is a self-limiting process: oxide created in the initial process forms a passivating skin over the remaining nitride material. The oxidation rate can be further retarded by pre-annealing nitride films, at approximately 1,200°C, in an inert ambient atmosphere. This preannealing process appears to reduce the reactive dangling-bond density in the film, as well as to increase the film's density.

**Silicon Oxynitrides.** These compounds are essentially amorphous polymers of Si, oxygen, and nitrogen of no definite stoichiometry. They can be prepared in a wide range of stoichiometries, with properties that bridge those of $SiO_2$ and $Si_3N_4$. These materials can also be engineered to retain the desirable properties of either the oxide or nitride films, without the drawbacks associated with the parent film. For example, whereas oxide films are usually under compressive stress, and nitride films are under tensile stress, oxynitride films can be engineered to be stress free. In PECVD oxynitride films, net stress depends on the frequency of *glow discharge*, which is plasma created by the action of magnetic and electric fields on gaseous materials.

Silicon-oxynitride films are deposited by a variety of techniques and chemistries, including those listed in Table I. For low-thermal-budget applications, silicon-oxynitride films can also be deposited at temperatures <450°C by PECVD or ECRCVD. The films deposited by these techniques are nonstoichiometric, however, and contain up to 20 percent hydrogen. If DCS ($SiCl_2H_2$) is used as the Si source, these low-temperature deposition films may also contain a relatively high concentration of chlorine.

Physically, silicon oxynitrides can be viewed as

two-phase mixtures: a highly ordered, nitride-like material, and a highly disordered phase domain of approximately 50 Å in diameter. Relative amounts of the respective phases depend on the Si-to-N ratio and hydrogen content. In final device passivation, the speed of sodium diffusion through silicon-oxynitride films depends on the relative ratios of the two film phases (discussed earlier). At temperatures up to 400°C, diffusion in the nitride-like domains has been reported to be much slower than that in disordered domains.

Physical and electrical properties of silicon-oxynitride films also depend on relative oxygen content. Oxygen doping degrades the nitride-like phase, thus reducing device-protection efficiency against mobile ions and scratches caused by the oxynitride film. Electrical resistivity, dielectric breakdown field, and the etch rate of ammonium-fluoride/hydrogen-fluoride buffer or mixture (BHF) all increase, while film stress, static and dynamic dielectric constants, refractive index, hydrogen content, and defect density all decrease with increasing oxygen content. Clearly, an oxynitride film of suitable composition for passivation and interdielectric applications can be engineered by balancing these properties.

**Undoped Silicon Dioxide.** $SiO_2$ films can be classified into two main groups, depending on whether the starting material used is inorganic or organic. Inorganic films are produced by thermal oxidation of Si or $SiH_4$, whereas organic precursors, such as organosilanes, are used in organic-based films. Chemistry and process conditions for depositing $SiO_2$ films depend on the intended applications (see Table I). For example, hydride-based ($SiH_4$) oxide films are inadequate for advanced VLSI and ULSI technologies, due to poor step-coverage of the as-deposited films.

Film-quality metrics, including conformal ability, intrinsic stress, density, and dielectric constants $(3.0 \leq \varepsilon \leq 9.0)$ of as-deposited $SiO_2$ films range from poor to excellent, depending on the process conditions employed in film deposition. The major difference between CVD and thermally grown oxides is the concentration of impurities, such as hydrogen and chlorine. CVD films tend to contain a higher concentration and wider variety of impurities, depending on the precursors used. Interestingly, contamination of CVD films does not drastically degrade the dielectric constant of these films, making it possible to use CVD oxides in place of thermally grown oxides in most applications.

Film-deposition kinetics differ between thermal oxidation and CVD, making films suitable for specialized tasks. For example, faster CVD film-deposition rates and lower processing temperatures facilitate thicker film formation for device passivation and interlevel insulating.

Thermally grown $SiO_2$ films have applications in many areas, including tunneling, gate, pad, masking, surface-passivation, and field oxides. The as-deposited $SiO_2$ film is amorphous, and has a random network of polyhedra with a net open structure. The open structure makes interstitial diffusion of impurities, such as $H_2O$, Na+, K+, Pb, Ba, P, and B, rather facile. These impurities also weaken the $SiO_2$ film's polyhedra-network structure.

Metallic contamination of such oxides is of primary concern to the integrity of gate oxide for advanced CMOS technology. Due to their ease of oxidation, oxides of metals, such as Fe, Mg, and Zn, are easily incorporated into $SiO_2$ films. Scrupulously removing these contaminants is very important, because the metal centers create traps and recombination sites in the dielectric film and degrade device performance.

Formation of $SiO_2$ films from the decomposition of liquid organosilicon Si precursors in CVD processes has come of age, and is epitomized by the use of TEOS, 2,4,6,8-tetramethylcyclotetrasiloxane (TOMCATS), and octamethylcylotetrasiloxane (OMCTS). In these processes, gas-phase reactions produce the reactive intermediate that subsequently decomposes to create the desired material. Surface reactions do play an essential role, however, depending on process conditions. In addition, defects and gas-phase nucleation are minimized in these processes.

Both CVD and thermally grown $SiO_2$, as well as the Si-to-$SiO_2$ interface, contain charges and traps that affect the electrical properties of the films and the devices fabricated from them. In general, the occurrence and density of charges and traps depend on the film-deposition technique and conditions—and in some cases, crystallographic orientation of the substrate.

$SiO_2$ films are typically under net compressive stress, due to differences in the coefficients of thermal expansion between film and substrate. This stress affects the applications of oxide films; stresses concentrate at sharp corners in features defined in $SiO_2$ films, and can enhance diffusion.

**Doped Silicon Dioxides (BPTEOS, BPSG).** CVD oxide films are easily doped by the introduction of appropriate

**Table I. Summary of process chemistry, deposition conditions, typical applications, and critical attributes of some dielectric-film materials for advanced VLSI and ULSI.**

| Film | Process Chemistry and Conditions | Typical Application | Critical Attributes |
|---|---|---|---|
| Silicon nitride | By APCVD from:<br>$SiH_4 - NH_3$ (700°C to 900°C, 1 atm) | Na, $H_2O$ barrier | Density |
| | By LPCVD from:<br>$SiCl_2H_2 - NH_3$ (700°C to 800°C, <500 mTorr)<br>$Si_2Cl_6 - 6NH_3$ | — | Hardness, and resistivity to Na and $H_2O$ |
| | By PECVD from:<br>$SiH_4 + N_2$ (200°C to 350°C) | Device passivation (encapsulation) | — |
| Silicon oxynitride (SiON) | By LPCVD from:<br>$SiH_4 - NO/N_2$, $SiH_4 - O_2 - NH_3$,<br>$SiH_4 - CO_2 - H_2 - NH_3$, and<br>$SiCl_4 - CO_2 - NH_3$ | Device passivation (encapsulation) | Properties of the deposited film depend on the $SiH_4$/oxidant ratio |
| | By reactive sputtering of Si:<br>$N_2 - N_2O$ or $N_2 - O_2$ | — | — |
| | By PECVD of $SiH_4 - N_2O - NH_3$ | — | — |
| Undoped silicon dioxide | By APCVD:<br>Si substrate + $O_2$ (or $H_2O$) (>900°C, 1 atm)<br>TEOS − $O_3$ (400°C to 700°C, ≤1 atm) | Gate/capacitor, isolation | Low defect, barrier |
| | By LPCVD from:<br>$SiH_4 + O_2$ (or $N_2O$) (500 mTorr, 700°C to 800°C)<br>TEOS (350 mTorr, 600°C to 750°C) | Premetal dielectric gap fill | Conformality |
| | By PECVD from:<br>TEOS, $SiH_4 + O_2$ (400°C), or TEOS + $O_3$ (400°C) | Interlayer/postmetal dielectric | Conformality |
| | By spin casting from:<br>SOG | Coat and bake | Fill |
| Doped silicon dioxide | By LPCVD from:<br>TEOS + TMB + TMP (650°C, 350 mTorr) | Interlayer/postmetal dielectric | Conformality |
| | By PECVD from:<br>TEOS + TMB + TMP (400°C, 350 mTorr) | — | — |

doping reactants into the film-deposition system. Doping decreases the $SiO_2$ film's melting point and thus its reflow temperature. For example, doped-glass films can be formed by the addition of phosphine ($PH_3$), trimethyl-phosphite ($C_3H_9PO_3$, TMP), triethylphosphite ($[C_2H_5]_3PO_3$, TEP), arsenic, diborane ($B_2H_6$), and trimethylborate ($C_3H_9BO_3$, TMB) vapors to oxide precursors. For safety reasons, the trend is toward the use of liquid-dopant sources.

The reflow temperature and other properties of doped films depend on dopant concentration and distribution. Dopant concentrations are easily tuned by adjusting the ratios of the dopant to the oxide-precursor gas-flow rates. Dopant distribution and film-thickness uniformity are controlled by varying the substrate temperature, process pressure, and load spacing in batch processes. Competing trends of planarization attributes and dopant segregation are such that optimal composition of
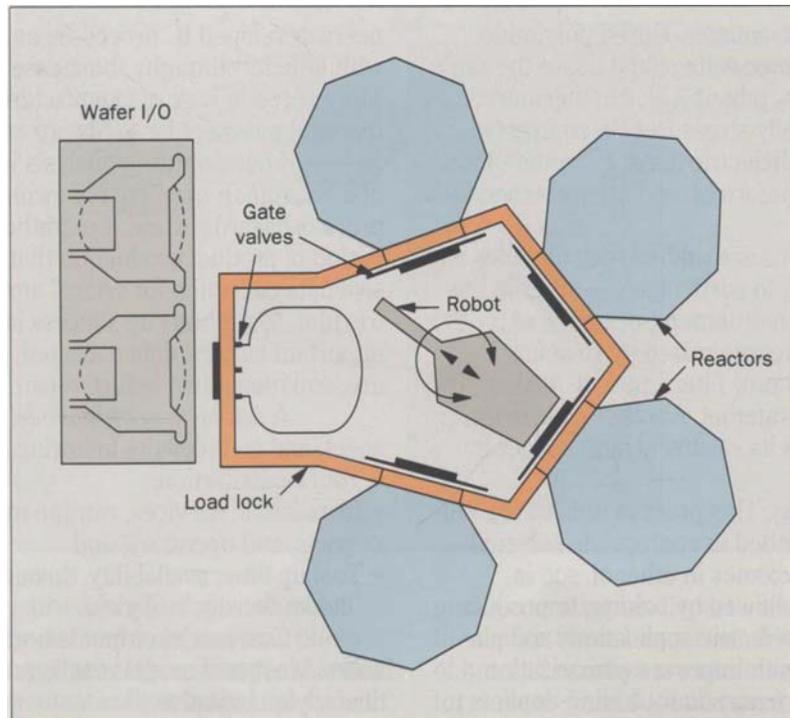
**Figure 2. Production reactors may be configured with load-lock chambers, which isolate the deposition chamber from the ambient atmosphere. This figure is a schematic representation of a typical cluster-tool platform with a single load-lock chamber feeding four reactors.**

doped-glass films depends on the aspect ratio and application. In general, the trend is to avoid excessive doping.

Deposition of doped oxides is problematic. Side reactions, gas-phase particle nucleation, and moisture in the reactor produce particulates that can be embedded in the films. Concentration of dopants at the film and air interface is a crucial parameter; above some critical concentrations, dopants tend to segregate into crystallites and react with room moisture to form globular masses, or stains, at step and pattern edges. Fortunately, many of these problems can be controlled with process optimization and prudent process integration.

The dielectric constant of organic-based $SiO_2$ films appears to be insensitive to doping level and deposition technique. In general, the dielectric constants of LPCVD films are about five percent lower than those deposited by PECVD. CVD films, irrespective of precursors, techniques, and doping, tend to contain fixed charges, which can cause $V_f$ shifts.

**Polyimides.** In addition to the stringent constraint of inorganic analogs, organic dielectrics must meet several other unique specifications if they are to be used in advanced VLSI and ULSI. For example, organic materials must not outgas, and they must be thermally and tempo-

rally stable up to 400°C. To avoid deforming underlying structures, these materials must have higher glass-transition temperatures than those used in subsequent processing, including packaging.

Polyimides are used as insulators, as planarizing layers to cover substrate topography, and as passivating agents. Purity of polyimide precursors is less than optimum with respect to metal contaminants, and diffusion of contaminants through even fully cured films is unacceptably fast. Thus, polyimide films are frequently deposited on $SiO_2$ or $S_3N_4$ barrier films. Adhesion of polymers to such underlayer films is generally poor, and a considerable amount of film-surface preparation is required by using coupling agents. Polymers are applied to the substrate surface in organic solvent solutions. Once cured, however, the polymers are not affected by the solvents. Bake temperature for full amidization is about 400°C. Solvent choice is dictated by polymer solubility, flammability, toxicity, coatability, and drying characteristics. Environmental considerations are driving development and use of aqueous-based systems. Viscosity of the coating solution must be low to facilitate filtration and dispensing, and yet high enough for spin coating.

Use of polyimide dielectrics in advanced VLSI

and ULSI offers several advantages. Cured polyimide films have a high breakdown voltage and about the same dielectric constant as $SiO_2$ (about 3.5). Furthermore, polyimide films are virtually stress free, in contrast to thermally grown or CVD dielectric films. Polyimide films are planar but not very conformal, and are patterned by a plasma-etching process.

Thin polymer films are riddled with pinholes and other defects due, in part, to particulates—either in the solution, in the ambient environment, or on the substrate. These problems are minimized by straining the solution through fine (0.2 μm) filters, and by flushing the substrate surface with a water jet. Another concern with the polyimide dielectric is its relatively high concentration of Na ($>10^{12}$).

**Spin-On Glass (SOG).** This process utilizes organo-silicon compounds suspended in appropriate solvents—for example, TEOS, and siloxanes in ethanol. SOG is applied by spin-casting, followed by baking, to produce $SiO_2$ films for interlevel dielectric applications and planarization. Doped films, with improved planarization attributes, can be formed from SOG by adding dopants to the casting solution. SOG-based oxide films have excellent thermal stability, low stress, good film uniformity, and superior adhesion to a substrate; they also have a lower degree of planarization when compared to polyimides and photo resists. Film-volume shrinkage, due to solvent loss, leaves the films under net tensile stress; carbon-based functionalities are introduced into the Si precursors to minimize cracking of the eventual SOG film. Resist-stripping solvents can degrade SOG films.

**Novel Dielectrics.** High-density DRAMs and other advanced application requirements (for instance, hot-carrier immunity) require a high dielectric constant and ferromagnetic materials. Examples of such materials include $Ta_2O_5$, $Y_3O_3$, $ZrO_2$, $Nb_2O_5$, and $HfO_2$. These materials are deposited by metal-organic chemical-vapor deposition (MOCVD) from their alkoxide and b-diketonate complexes, by photo-CVD, rapid-thermal-anneal chemical-vapor deposition (RTACVD), and LPCVD, to provide excellent step-coverage for trench and stack-cell structures.[8,9]

### Film-Deposition Hardware

Economics play an important role in hardware selection for most IC processes. It is no longer acceptable to show small improvements in the level of integration at any cost. In the past, research scientists and engi-

neers developed IC processes on laboratory-grade tools, with little forethought about ease of manufacturing. More recently, ease of manufacturing has become the primary requirement for hardware and process selection.

Manufacturing analysis is completed by means of a "*marathon run*," cost-of-ownership modeling, and a process-hazard review. A marathon run is an extended period of product production that is monitored by passive data collection for critical attributes about a dielectric film. Marathon-run success is measured by three important factors: data collected, mean time before failure, and mean time before repair.

A *cost-of-ownership model* is typically a spreadsheet, and includes the following cost data:
- Tool capitalization;
- Installation, services, routine maintenance, spare parts, and operators; and
- Tool up-time, availability, throughput, wafer value, defect density, and yield.

Cost-model output is normally stated in cost per wafer. Most cost-model results are relative, and not particularly quantitative.

A *process-hazard review* is a "what if" meeting of operators, maintenance personnel, and engineers in facility planning, environmental safety, development, and manufacturing. Most deposition processes use toxic, poisonous, flammable, or caustic materials. Furthermore, high temperature, high electrical power, radio frequency (RF) or microwave energy, and magnetic fields are sometimes used. Mechanical risks of robotics and automation are ever present. The committee studies all of these potential hazards, plus appropriate methods of diluting, scrubbing, and disposing of process effluents.

Fundamental tool requirements for coated and CVD dielectric materials are quite different. Tools for coating polymers are usually automated, in-line track systems. As the tooling dispenses liquid dielectric material, a wafer is rotated at several thousand revolutions-per-minute to spread the material evenly across the wafer's surface. The coating process also requires a series of baking steps. An oven can be either part of the same track tool or a separate facility.

CVD tool requirements include:
- A controlled chamber, with energy for reaction;
- Gas control, metering, and delivery manifolds; and
- An exhaust system to deal with reaction effluents.

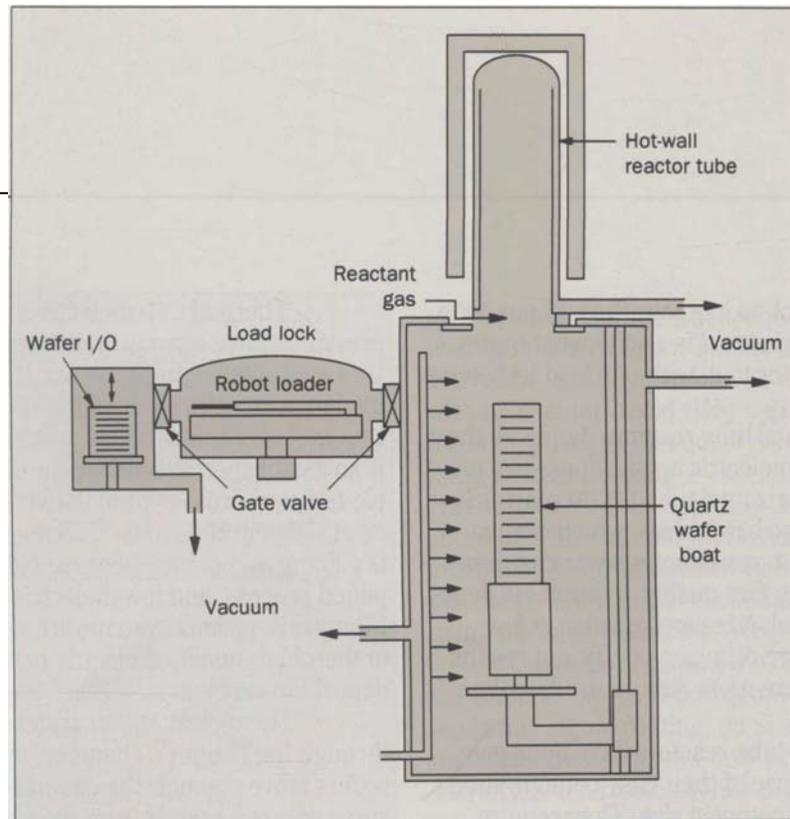A CVD reaction chamber has both a tempera-

Figure 3. Hot-wall, vertical-tube reactors have been gaining popularity because of their automated operation and small "footprint." This schematic shows the components of a commercially available, vertical, LPCVD hot-wall tube reactor.

ture-controlled and pressure-controlled environment. Reaction energy could be derived from thermal, photochemical, or glow-discharge processes. The gas manifold typically incorporates pneumatically actuated valves with stainless steel bellows seals, high-precision mass-flow controllers, electropolished stainless steel tubing, gas purifiers, and filters. Exhaust-system requirements are dictated by reaction pressure. For example, low-pressure deposition requires a vacuum pump, configured with a roots-type blower, for extensive ventilation. Atmospheric-pressure systems, needing only minimal exhaust, do not require forced-air ventilation.

Reactors can be classified as hot wall or cold wall, low pressure or atmospheric pressure, and by reaction kinetics—for example, thermal or plasma. LPCVD processes range from 0.05 Torr to 90 Torr (1 atm = 760 Torr). Temperatures for thermal reactions range from 100°C to 1,000°C. RF or microwave plasma, as well as atmospheric-pressure process temperatures, typically range from 350°C to 500°C.

Dielectric films tend to be deposited on reactor hardware. It is important to understand the nature of these deposits, because they actually represent part of the reactor chamber. While films deposited on hot-wall reactor walls are similar in quality to those deposited on a substrate with good adhesion, the deposits on cold-wall reactor walls are low-quality, porous films having minimal adhesive strength.

Films deposited on cold walls tend to crack and

peel, generating small particles that may become part of the device films. In contrast, films deposited on the walls of hot-wall reactors are more tightly bonded to the reactor walls and are difficult to remove. When deposits on the hot walls exceed some critical thickness, they crack, producing particles that "kill" yields.

In some reactors, the wafer is rotated or oscillated to improve film-deposition uniformity. A variety of schemes is used to introduce reactants and diluent to the chamber. In tube systems, gases are usually introduced from the source end of the tube. Injectors may be used in tube reactors to improve within-batch uniformity. Typically, "pancake" batch reactors either have gases introduced at the center or at the periphery of the platen. The gases are then directed across the wafer's surface. Single-wafer PECVD or APCVD reactors introduce gases through a dispersion head, located close to the device side of the wafer.

Production reactors may be configured with load-lock chambers, which isolate the deposition chamber from the ambient environment. In this scenario, the process chamber is maintained at base pressure, while wafers are loaded into the load lock. Then, the load lock is "pumped down" to the same base pressure as the deposition chamber, and a gate valve is opened to accept wafers into the process-deposition chamber. The gate valve is then closed. After the deposition process is completed, wafers are removed by reversing the same procedure. Systems may have multiple load locks or multiple

chambers off one load lock to increase throughput, as in the cluster-tool concept. Figure 2 is a schematic representation of a typical cluster tool, with one load lock serving four reaction chambers.

Hot-wall, horizontal-tube reactors dominate the Si IC industry for LPCVD dielectric applications. The primary advantage of the horizontal-tube LPCVD reactor is its accommodation of large batch sizes, which dramatically increases throughput, resulting in lower cost processing without sacrificing film quality. Reasonable deposition rates with large batch sizes are possible at low pressure, because the large diffusion coefficient results in surface reactions that are more rate controlling than mass-transfer processing.

Hot-wall, vertical-tube reactors have been gaining interest recently because of their easy configuration for automatic loading and compact size. They require less clean-room floor space, which is usually scarce. They also produce more uniform films than horizontal reactors. Figure 3 shows a typical, commercially available, vertical LPCVD hot-wall tube reactor.

Advantages of LPCVD reactors include:
- Uniform step-coverage,
- Precise control of stoichiometry,
- Lower-temperature processing,
- Higher deposition rate,
- High throughput, and
- Low cost.

The typical LPCVD reactor consists of a quartz tube heated by a multizone furnace, with reactants introduced at one end and pumped out the other. LPCVD process pressures range from 0.25 Torr to 2.0 Torr. LPCVD process temperatures range from 300°C to 900°C. Wafers are positioned perpendicular to the main direction of reactant flow and are supported concentrically inside the tube. Gas flows range from 100 standard cubic centimeters per minute to 10 standard liters per minute. Special inserts are sometimes used in the reactor to disperse and distribute the gas, as well as to change gas-flow direction.

A typical LPCVD reactor consists of four regions or zones: premix, preheat, wafer, and downstream. The preheat and downstream zones are empty tube sections, located immediately before and after the wafer region. Gas-phase reactions in the preheat zone may influence growth on the wafers, while the downstream zone appears to have a negligible effect on the wafer region.

Thermal CVD dielectrics at atmospheric or low pressures have serious limitations for advanced VLSI and ULSI applications. In particular, thermal budgets dictated by device structures, silicides, and metalization schemes require lower-temperature processing. Glow discharge is an established alternative for deposition at lower sample temperatures. Typical PECVD reactions are completed at temperatures <400°C. Spin-on coating of polymers is gaining acceptance because of lower capital cost, simplified process, and low-dielectric-constant materials. Microwave plasma systems are also of interest because of their high-quality dielectric materials and directional deposition capability.

The typical APCVD system carries wafers through the reactor's chamber on a conveyor belt. As wafers move through the chamber, overhead injectors spray gaseous reactants on the wafers as the substrate passes beneath the injector nozzles. Inert gas curtains contain the reactants, and convection heats the substrate. The advantages of this type of reactor are high throughput, good uniformity, and the ability to accommodate various wafer sizes with minimal retrofit cost.

The radial-flow, parallel-plate, cold-wall PECVD reactor has a cylindrical chamber. Wafers are placed on the lower electrode, which is grounded. An RF potential is applied to the top electrode to strike the plasma. RF, applied across electrodes, is used to generate magnetic and electric field modulations to ionize gaseous reactants in the reactor. Gases flow radially through the discharge, usually from the outer edge toward the center, but the opposite flow direction is sometimes used, depending on design preference. The grounded electrode is heated to a temperature between 100°C and 400°C by resistance heaters or high-intensity lamps. This procedure's main advantage is its low deposition temperature and good uniformity. Disadvantages include lower throughput, and particulates from loosely adhering deposits sticking to the cold reactor walls.

Single-wafer reactors for APCVD and PECVD have the inherent advantage of more confined reaction, which lends to process tailoring and automation. Highly localized reactions can be used to modify very small substrate areas. Single-wafer systems have lower defect densities because of their smaller volume and resultant lower gas-phase nucleation. The typical single-wafer reactor has a gas flow normal (90°) to the substrate's surface.
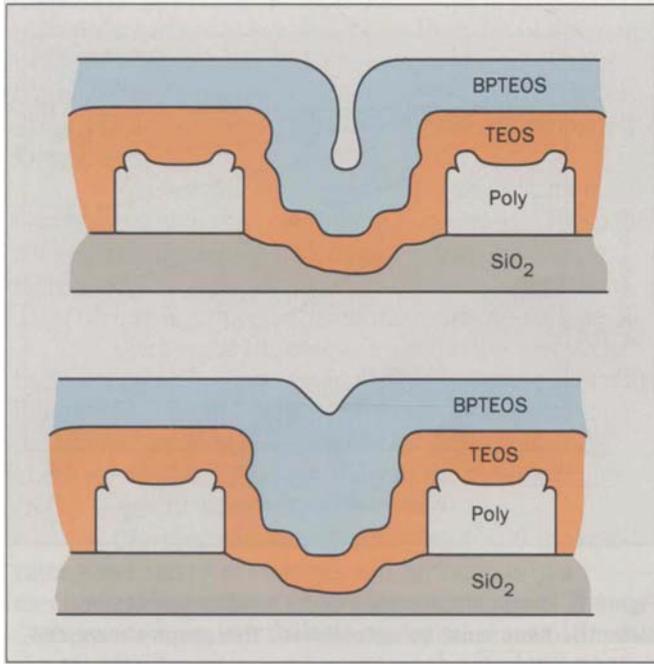
**Figure 4. Dopants can be added to oxides to lower their melting points. This illustration shows cross sections of conventional, doped-oxide materials before and after high-temperature annealing.**

Typically, LPCVD and PECVD reactor chambers and their gas-delivery manifolds must be vacuum tight. Materials frequently used to construct CVD reactors include quartz, Al, stainless steel, graphite, ceramics, and high-temperature plastics. Gas-delivery lines are typically welded, or use vacuum-compressed-ring (VCR) soft-metal gaskets and anti-torque connectors. Hard-surface interfaces exposed to reaction are sealed with advanced polymer o-ring materials, such as Kalrez or Teflon-encapsulated Viton (Kalrez, Teflon, and Viton are registered trademarks of E. I. DuPont de Nemours).

Most production systems are operated by menu-driven software. There can be hundreds of digital and analog inputs to a system that sense process variables, position of indicators, gas flows, temperatures, pressures, and a variety of other parameters. Most software includes safety interlocks as well. Usually, several different process recipes are stored in memory.

CVD reactors require periodic cleaning. In general, hot-wall reactors are disassembled for cleaning because materials deposited on the reactor's walls are

well bonded. Materials deposited on the walls of a cold-wall reactor are of poor quality and do not stick well. Therefore, the deposits can be cleaned easily, in situ, with hydrofluoric acid (HF) vapor or plasma discharge of freon. In terms of film quality, uniformity, and particulates, reactor cleaning is essential to process consistency. Hot-wall reactors are typically cleaned with diluted HF solution, whereas cold-wall reactors are cleaned with alcohol or de-ionized water. Recent developments in RF-discharge and thermal cleaning of hot-wall tube reactors, using nitrogen trifluoride ($NF_3$), are very effective.

**Integration Schemes.** IC fabrication requires defining multiple layers of fine geometries, for active components and signal routing, on Si substrates. Thin dielectric materials are useful, not only as insulators, but also as sacrificial etch masks. While dielectric-insulator levels are clearly depicted in the cross-sectional illustration (Figure 1), sacrificial materials are removed early in processing. Furthermore, most dielectric layers appearing in the cross section incorporate complex integration schemes to meet individual device requirements.

Common integration schemes include:
- Hard masking,
- Ion-implant screening,
- Isolation masking,
- Reverse-via processing,
- Gate spacing,
- Filleting,
- Resist-etchback integrating,
- Block-resist patterning,
- Chemical-mechanical polishing,
- Damascening,
- Gap filling, and
- Flowing and reflowing.

The latter six methods are planarization or smoothing processes to address topography concerns.

*Hard-masking* is used as an RIE mask, where increased line-width control is required. Historically, photosensitive polymers have been used to define patterns, and as etching masks for pattern transfer to deposited polycrystalline Si or Al films. Recently, researchers found that photosensitive polymer materials cause loading effects in RIE plasma, which lead to uneven etching of dense areas as opposed to open areas. Hard-mask material is deposited directly on the material to be patterned. Then, the photosensitive polymer is applied and defined. Used first as a mask to etch the hard-mask

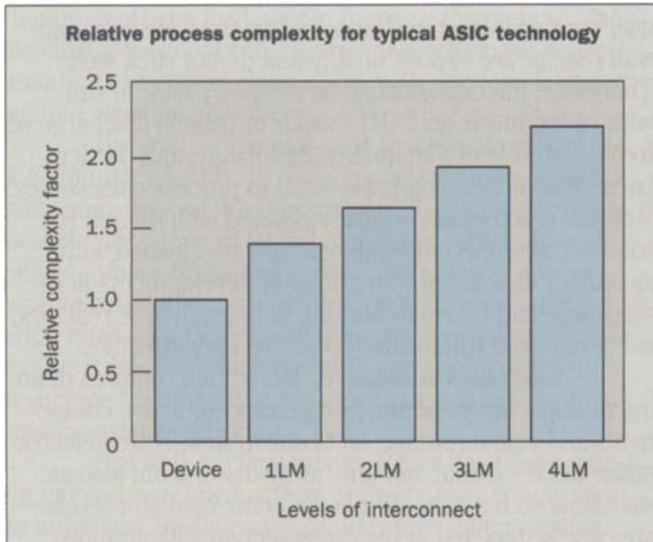**Relative process complexity for typical ASIC technology**

Figure 5. In advanced VLSI and ULSI devices, higher levels of integration place greater demands on dielectric-material processing. This bar graph shows the effects of IC-technology complexity on interconnect, relative to active device circuitry.
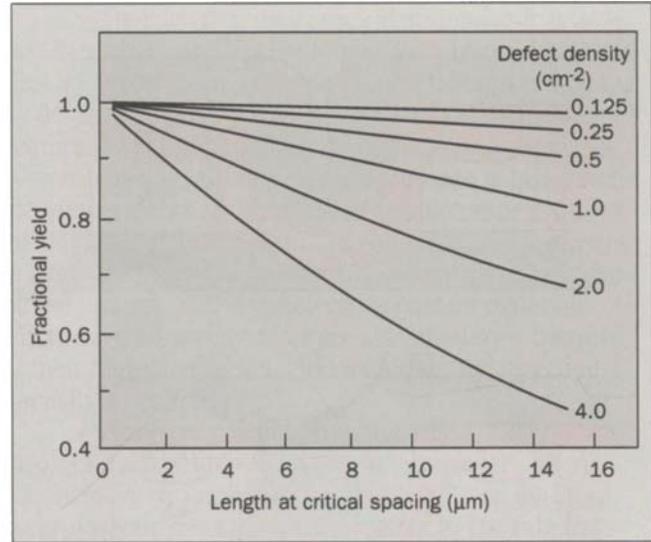


Figure 6. Measuring techniques for smaller defects in dielectric films must be established. This graph shows estimated fractional yield loss to conductor trace length, at critical design rules, by defect density at sub-one-half-micron geometries.

material, the patterned polymer is then removed, and the hard mask serves as the mask for actual polycrystalline Si or Al etching. Subsequently, the hard mask is removed.

*Ion-implant screening* is an integration scheme that uses a dielectric material overlayer, such as $SiO_2$, to retard ion penetration. The typical screening film is sacrificial and is removed after use.

*Reverse-via processing* is an effective method for contacting fine features—without sacrificing metal step-coverage in the window—by creating a tapered window profile. The reverse-via process starts by defining window patterns, and proceeds through directional anisotropic RIE window-pattern transfer. The anisotropic etch is terminated partially through the dielectric. Then, the photosensitive polymer is removed and dielectric etching is continued with a partially isotropic and partially anisotropic RIE plasma. The upper portion of the window becomes wider as the bottom of the window nears the contact point. This approach results in local smoothing of the top dielectric surface.

Dielectric smoothing and planarization become essential as device integration increases and geometries enter sub-one-half-micron size. Most smoothing or planarization processes require additional thicknesses of

deposited dielectric. Final dielectric thickness is predicted by device requirements. Photolithographic depth-of-focus requirements are becoming extremely tight for advanced technologies. Dielectric smoothing—and ultimately, planarization schemes—play an important role here. Resist-etchback planarization uses photo resist to fill undulations in the dielectric, and then isotropic RIE chemistry—with similar dielectric material and resist etch rate—is used. The block-resist process prints sacrificial resist patterns in trench, or low-lying areas, followed by a similar isotropic etch.

*Gate spacing* and *filleting* basically form a tapered side wall on existing features. This process is referred to as *spacer*, and serves as a source/drain-to-gate spacer for lightly doped ion-implant masking. Filleting is the term used in back-end processing. The spacer or fillet is created by depositing thick dielectric films and anisotropically etching them back. Typically, 40 percent to 70 percent of the deposited material is etched back. The spacer forms at areas where the side walls are masked from much of the RIE chemistry.

Argon sputtering is sometimes used to form fillets at interlevel metal-dielectric processes, in which argon is ionized in a plasma. The ions then bombard the

material's surface to break it loose. Because of the magnetic fields associated with the ions, argon sputtering could be very anisotropic. The process removes material very selectively at corners in a ratio of approximately four to one, resulting in a roof-top profile.

*Resist-etchback integrating* is a planarization scheme in which resist is spun onto a surface. Then, the resist is reactive-ion etched, using a chemistry with an etch rate as close as possible to the underlying material. The polymer is stripped off, leaving a smooth surface.

*Block-resist patterning* is similar to resist-etchback integrating. However, in the block-resist-patterning integration scheme, the areas for etch-back smoothing are defined by photolithographic methods, and an RIE chemistry with higher selectivity to the dielectric film ($SiO_2$) is used.

*Chemical-mechanical polishing* (CMP) incorporates a wet slurry of etchants and surfactants in a mechanical lapping tool for global planarization. The CMP process requires delicate control of removal depth.

*Damascening* incorporates advanced schemes of metal plug and CMP. After a dielectric is deposited, trenches are etched with conductor-trace and contact-window patterns. The trenches are subsequently filled with a conductor material. The structure then gets CMP, several thousand angstroms into the dielectric, to ensure there is no chance of a short circuit.

*Gap filling* is the term used when high-aspect-ratio trenches are filled with a low-quality material. Conductors are coated with a quality dielectric. Then, a lower-quality filling material is deposited, such as spin-on glass or APCVD $O_3$-TEOS. Isotropic etchback leaves low-quality material in the trench areas. Subsequently, this material is capped with a more dense and less hygroscopic layer. In this scheme, windows are not patterned through the low-quality fill material. It is advantageous to perform vacuum bake-out of the low-quality material before the second deposition in situ.

Dopants can be added to oxide materials to lower the temperatures at which the oxides melt. Two commonly used dopants are boron and phosphorus. Phosphorus-doped oxides typically flow or melt at temperatures above 950°C at >4 wt% P. Complex boron-phosphorus-doped oxides will flow or melt at temperatures as low as 800°C, at ~4 wt% P and 4 wt% B. Figure 4 shows a cross section of as-deposited and post-anneal profiles of BP-doped oxide film over polysilicon features. Germanium and arsenic dopants have also been shown

to lower the melting point of oxides.

*Flowing* and *reflowing* are processes that smooth and round edges by melting material at high temperature. *Reflow* is a term used to describe a flowable material with a contact window cut. The upper edge of the window may be rounded by reflowing the glass to improve drastically the step-coverage of the metal.

### Dielectrics in Advanced VLSI and ULSI

Higher levels of integration place greater demands on dielectric-material processing. Aspect ratios increase, and the thermal budget decreases, as device geometries shrink. Furthermore, levels of interconnect and length of interconnect routing also grow with an increase of device functions. Figure 5 shows process complexity versus impact of multilevel interconnect technology. Basically, back-end interconnect and interlevel dielectric processes become more complex than the device levels at four interconnect levels. Advanced VLSI and ULSI technologies at sub-one-half-micron geometries mandate greater than four levels of interconnect. For advanced device functions, there will soon be six to eight interconnect levels.

The base-line 0.5µm CMOS process used within AT&T Microelectronics incorporates three levels of metal interconnect, and the initial 0.35µm CMOS technology uses four levels of interconnect. Enhancements to older technologies, such as 0.7µm and 0.9µm CMOS, will drive circuit area down, yielding increased speed by migrating from two-level to three-level and four-level interconnect technologies.

The aspect ratio of conductor height, divided by the spacing between conductors, is a primary concern for advanced VLSI and ULSI dielectrics. Furthermore, lithographic requirements of advanced IC technologies require relatively planar surfaces to accommodate decreasing depth-of-focus and pattern distortion.

Measuring techniques for smaller defects must be established. Defect-density requirements will drop dramatically for advanced VLSI and ULSI. Figure 6 shows the estimated fractional yield loss, versus conductor trace length at the critical design-rule spacing, for cumulative process-defect densities from 0.12 $cm^{-2}$ to 4.00 $cm^{-2}$. It is clear that submicron, design-rule-size defect densities below 0.5 $cm^{-2}$ are required for moderate, completed device yields.

New low-dielectric-constant materials for tighter spacing are required to control RC time constants for

increased device speeds. These new materials must also meet all the requirements of older technologies. Lower thermal budgets, resulting from shallower junctions and the use of thin silicides, will place constraints on reaction kinetics. Devices will become much more sensitive to charge damage.

More robust materials and reliability considerations will be paramount for a competitive edge. Economics will dictate increased tool and process longevity. Manufacturing ease and lower cost-of-ownership on larger-diameter substrates will also be keys to success.

## Summary

As device sizes shrink and ICs become more complex, the demand for reliable dielectric materials will increase. Dielectrics are as reliable as their judicious application. Thus, the capabilities and limitations of the available material systems must be understood. Specifically, an understanding is required of the relationship between the processing techniques and conditions, as well as the physical, chemical, and electrical properties of the materials. For example, in order to effectively and judiciously use these materials in designing products, engineers must understand the effects of electric fields and current on the thermodynamics and kinetics of solid-state processes in thin films.

In advanced VLSI and ULSI, dielectric and insulating materials are used in a variety of applications, such as insulators, diffusers, implants, and etching masks, as well as in final passivation. The stringent demands on such films require a clear understanding of the dielectric and insulating materials used in these technologies, the deposition processes, and the hardware. Accordingly, dielectric and insulating films were discussed with regard to materials, material-deposition chemistry, physical properties, and device applications. Films deposited by PECVD and LPCVD processes, as well as spin-cast (SOG and polyimide) techniques, were presented. References were also made to emerging dielectric materials and film-deposition techniques.

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