Manufacturing Issues of the 1B Processor

Lisa A. Flynn
Thomas M. O'Leary

This paper outlines the critical strategies, facilities, and processes put in place to meet the high reliability and quick ramp-up requirements of manufacturing the 1B24 processor. The intent is to provide insight into several of the functions necessary to support the project objectives, including organization, vendor involvement, contingency planning, stocking, testing, and processes.

Manufacturing Overview

With the planned introduction of 1B24 processors into 134 AT&T 4ESS™ switch offices, it was imperative that manufacturing develop a highly focused, tightly controlled production process that could provide for contingencies without affecting this aggressive year-long deployment schedule.

This deployment, three times faster than any previous network deployment plan, called for four office cutovers at a time, typically on a weekend, without affecting network traffic in any way. It was manufacturing's responsibility to have the 1Bs ready, when and where they were required.

Due to this stringent deployment schedule, a single manufacturing operation organization was created to span both engineering and operations. Certain support operations, such as material presentation, stores, and common production planning remained within their regular organizations, although they were appropriately "matrixed" to the 1B24 manufacturing effort to meet the project requirements.

The manufacturing plan had three major project phases: prototype, preproduction, and production. Manufacturing, of necessity, became the cornerstone of successfully completing the project in the production phase. All project participants, including the customer, helped to iteratively mold the plan through all three project phases.

The three key manufacturing parameters were:

- Achieve high yields ahead of the production ramp,
- Have contingency plans for potential obstacles, and
- Miss no ship dates,

Three fundamentals that guided manufacturing were *focus*, *people engagement*, and *structure*.

Creating a Tight Manufacturing Focus.

Keeping a tight focus on manufacturing efforts was accomplished in two principle ways:

- Organizing an independent manufacturing shop in the Columbus Works that was dedicated only to the 1B24 program. The shop was a contiguous operation that fabricated all elements of the 1B24 processor and its conversion switch, which was used to switch the 4ESS switch from the 1A processor to the 1B processor.
- Creating a single organization, headed by one individual, to which both operations and engineering reported, and to which support operations were appropriately matrixed.

This tactic clarified both assignments and their execution, localized the resolution of problems, and provided distinct accountability. Further, this focus gave clear signals to the customer, AT&T Network Services, of AT&T Network Systems' project commitment and control.

Engaging Manufacturing Personnel.

From the time the first technical and production associates joined the team, their own individual roles were accentuated and reinforced, while they also were informed on a regular basis about all aspects of the project

Panel 1. Abbreviations, Acronyms, and Terms

ATP — automated test process
CMOS — complementary metal-oxide semiconductor
CPFT — circuit-pack functional test
DFT — design for testability
ESS/T — environmental stress screening/testing
EST — environmental stress test
FMA — failure mode analysis
FSTEST—functional system test-environmental stress test
GSLM — AT&T Global Supply Line Management
ICT — in-circuit test
IOP — input/output processor
ISO 9002 — International Organization for Standardization model used for quality assurance in production and installation
ITP — integrated test process
KLW — manufacturing term for randomly generated designators for a particular circuit-pack profile.
PLD — programmable logic devices
STRIFE — stress to life

criticality, status, and performance. The manufacturing management team followed a high-visibility "being there" management style, maintaining a deliberate, continual presence at the work location. This style was based on the belief that employee empowerment and engagement not only come from formal communications but also from top-down and bottom-up interactions among all participants. Another dimension of engagement was the assignment of a physical designer and a circuit designer to Columbus for one year, beginning late in the preproduction phase and continuing throughout production.

Four technical managers were under one department head to manage four critical phases: operations/process engineering, test development and engineering, product engineering, and program/material management. This approach permitted rapid, precise decision-making and execution throughout the project, as well as guaranteeing the participation of the appropriate people in those decisions.

Under the operations manager, a group of floor superiors headed operations for a primarily two-shift, five-day work week, while an additional supervisor monitored the entire end-to-end span of the operation, as well as being the single interface with product engineering. The success of this tactic cannot be overemphasized, for it provided a mechanism for the floor supervisors to maintain teamwork and order, and to keep a tight focus on the workload.

A quality plan architecture was designed that consisted of two "cell teams," circuit pack and equipment. These teams received from the Columbus Quality Information System database information that was generated daily through quality sample monitoring. In addition, these two teams were supported by two process management teams, circuit pack assembly and circuit pack functional test, both comprising manufacturing engineers and designers.

Designing a Manufacturing Structure. The main manufacturing operation occupied approximately 30,000-square feet of contiguous space. Orientation was tight and deliberate, providing both an efficient flow of material, and the capability of flexibly handling a variety of potential anomalies and disruptions. The primary objective was not the speed of manufacture, but to provide a steady stream of output, integrated with deployment plans, and engineered so that any unexpected problems could be handled efficiently, thus protecting both the rollout and the customer's needs.

The objective was to be able to react quickly to emergency changes in circuit packs and to provide the flexibility to reconfigure the assembly line as needed. The fundamental circuit-pack line used a large "U"-shaped layout for contemporary reasons, and rolled back on itself, permitting, for example, the floor feedback points to be close together and the circuit-pack test/repair to be juxtaposed with integrated circuit (IC) programming.

The entire 1B24 manufacturing operation was ISO 9002 certified during the very early stages of production and was able to achieve a score of 97 percent on a stringent internal audit. As always, adhering to this type of discipline further helped the operation achieve its primary goals.

Strategic Positioning

This section will discuss some of the key factors in the effort to strategically position manufacturing in the product realization plan.

Contingency Planning. It was decided to start production early and to maintain a "build-ahead" stock of

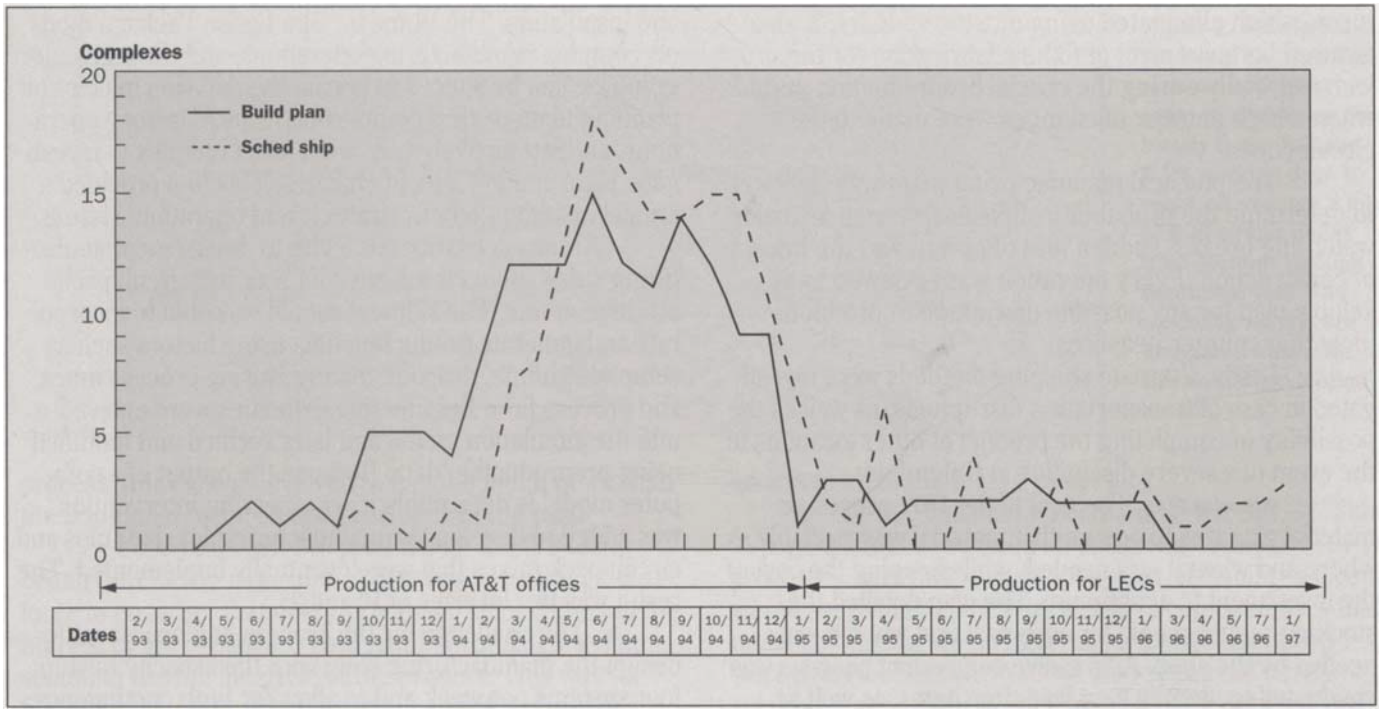

Figure 1. To maintain a "build-ahead" stock of processors throughout the life of the project, 1B processors were completed about six to eight weeks prior to delivery to the customer. This period provided sufficient time to deal with unforeseen problems, such as vendor supply delays, manufacturing and test issues, and schedule rearrangements.

processors throughout the life of the project. Processors were completed about six to eight weeks prior to delivery to the customer (see Figure 1). This period provided sufficient time to deal with unforeseen problems, such as vendor supply delays, manufacturing and test issues, and schedule rearrangements. In at least two instances, unforeseen problems did arise and the build-ahead program provided time for the problem to be resolved without affecting the customer.

As a safeguard against design changes and unforecasted product demands, a "safety stock" of components was defined to include enough circuit packs for eight systems and equipment and cables for seven systems. In addition, a completed circuit-pack safety stock of five systems also was available to provide time to respond to any emergencies without affecting shipping schedules.

The safety stock material remained at Columbus and was managed by the 1B24 program management team until all processors were in service. At that time, the material would be made available for general consumption by other programs at Columbus, such as building 1Bs for local exchange carriers, expanding 1B memory, building 1Bs for life stock, or meeting new 1B requirements.

Most of the facilities were planned on a five-day, two-shift work week and were to produce four processors per week. With the build-ahead stock, the actual schedule required only three processors per week, resulting in a 25 percent capacity reserve on the line, if needed. Also, a third shift for most operations was not needed, but was available if required.

All unduplicated equipment, such as the circuit-pack solder machine and radial-and-sip insertion machines, were carefully evaluated and a preventive maintenance plan was followed. Agreements were made, and a trial run was made with other shops to perform 1B24 work in the event of an emergency. An in-house fixture lab was used to provide HP3070 in-circuit test fix-

tures, which eliminated using outside vendors. It also assured better control of fixture fabrication for the project, especially during the crucial preproduction period, when a high number of changes were made to the circuit packs.

The physical manufacturing plant was reviewed to determine the probability of disasters, such as major water line breaks, sudden loss of power, and the impact of construction. Every operation was reviewed to develop a plan for any possible disruption to production, including countermeasures.

Lastly, alternate shipping methods were investigated in case of transportation disruptions, as well as the possibility of completing the product at other locations in the event of a severe disruption at Columbus.

Material Plan. The goal of the 1B24 processor material plan was to ensure that material was available where and when it was needed, while keeping the cost of the investment to a minimum. The plan detailed the stocking requirements for each part and when it was needed by the shop. Aggressive component analysis was conducted to identify long lead-time items, as well as those parts coming from small vendors. Reducing lead time was critical for this project, considering the volatility of early design changes. To support an accelerated change notice plan, special considerations were made to ensure that sufficient stocks of material were available.

Supplier Relationships. The success of the 1B project required close communication with suppliers. Project details and critical dates were shared at supplier conferences, where it was stressed to suppliers that problem-solving was as important to the project as on-time delivery. Suppliers were coaxed to openly share their process data with the 1B24 project team, and supply forecasts were frequently verified. Suppliers also were encouraged to surface problems with the team as soon as possible.

The environmental stress screening and testing (ESS/T), which the manufacturing process placed on components, was sometimes greater than that of the vendor's process. If a problem was found with a product, the supplier was asked to be open to an intensive, and highly disciplined, technical evaluation by both the vendor and the team.

Simulation Modeling. Computer simulation allowed the 1B engineering team to design, trial, and modify the manufacturing layout in advance of facility acquisition and installation. The Witness™ Simulation Package models complex manufacturing operations, and through color graphics, can be altered to permit the decision makers or planning team to view complex patterns of factory operations, and interactively use "what-if" techniques to investigate, plan, and implement changes. This tool provided a critical insight into both strategic and operational issues.

Many scenarios were run to determine manufacturing rules about circuit-pack lot size and circuit-pack production mix. The Witness model was able to incorporate and generate production data using factors such as setup, downtime, dropout, manufacturing process times, and process flow. Engineering estimates were entered into the simulation model and later verified and modified using preproduction data. Because the output of a computer model is deterministic, engineering intervention was added to develop the manufacturing lot size rules and circuit-pack mixes that were eventually implemented. The result was two lot sizes of 10 and 25.

The challenge for the process engineers was to design the manufacturing shop with the capacity to ship four systems per week and to allow for both contingency and predicted design changes. Simulation modeling enabled the process specialist team to integrate their individual processes and create a streamlined material flow. The manufacturing capacity of each manufacturing process, as well as the entire integrated process, was then able to be analyzed. Modifications were made to eliminate bottlenecks and, thus, optimize the entire process. The readily available data provided by computer modeling allowed all process engineers to more easily view and understand their impact on the big picture.

Simulation modeling is very structured and requires very specific data to create a useable and realistic model. The data-gathering phase and model construction phase is grueling and requires many decisions to be made and verified early in the manufacturing process development. The need for an early discussion of such topics facilitated decision making in the areas of product flow, handling of defective material, employee staffing, and material handling methods. Figure 2 compares the modeling results with the actual production results.

Integrated Test Process. The integrated test process (ITP) is a discipline by which a 100 percent test coverage strategy is defined and assessed by a joint manufacturing and design team. In the case of the 1B24

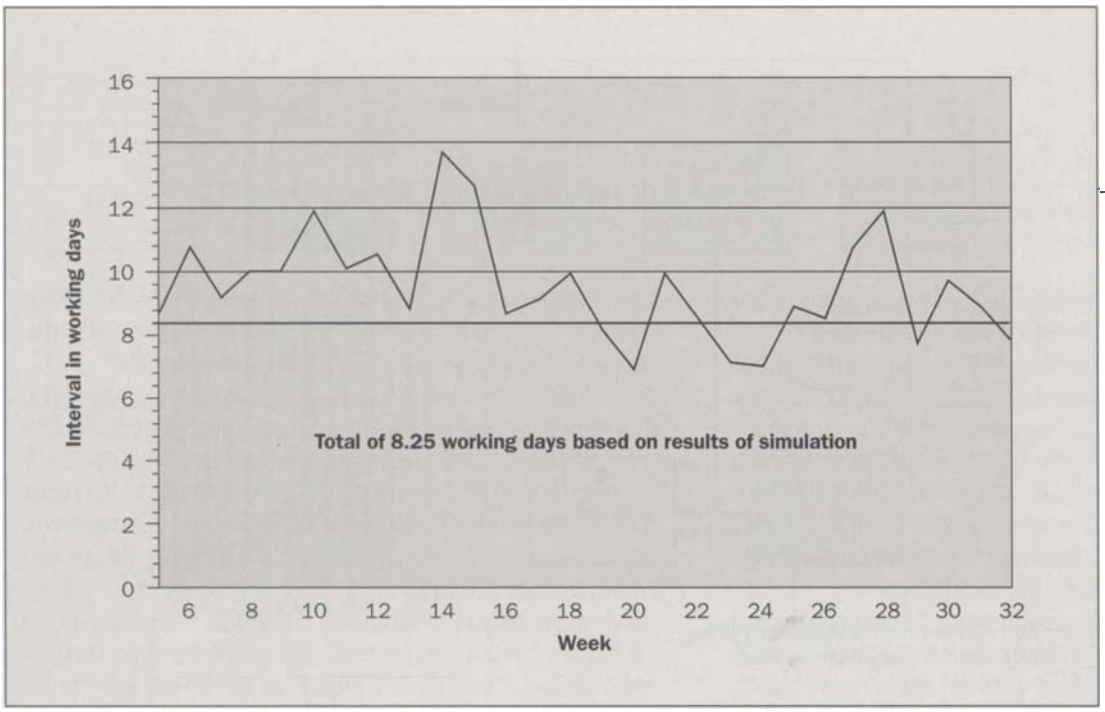

Figure 2. Simulation modeling enabled the process specialist team to determine that ideally it should take 8.25 working days to move on average a mix of 800 circuit packs from preform through functional test. The modeling results are compared here with the actual production results.

process, this concept evolved to include much more than the traditional focus on test processes of the past.

Four years prior to production, the ITP team began developing a document that was to be the guiding force in ensuring that every processor shipped was of the highest quality possible. This group formulated a plan spanning the full life cycle of the product. This was the first time the process had been expanded to detail every verification step necessary—from a component's entry into the factory to deployment of the product to the field.

The intent was total coverage of every aspect of product flow from in-the-door through long-term field support. This was achieved by establishing four subteams, each responsible for a phase of the manufacturing life of the product. Each team detailed the product flow, identifying every test, inspection, verification, and quality assurance point the product encountered. Every process explicitly listed its suppliers, customers, and deliverables, as well as what that particular functions could and could not be covered within the test/inspection process. The core team ensured there was no duplication of effort among the teams, as well as that there were no holes in the overall test process.

The concept of "product-tests-product" was a major ITP strategy. This meant that the processor hardware and software would be designed to test itself in the manufacturing and deployment processes. Any special test hardware or software also would be treated as product, ensuring long-term support of the hardware or software in question. Factory and installation tests were to be the same. Although the complete set of tests may not be used in both places, this ensures that everyone has access to all of the tests if necessary.

The ITP test plan was issued in March 1992. This 95-page document outlined all design-for-testability (DFT) processes, schedules, and capabilities. Reliability aspects were covered in depth. Which critical components would undergo ongoing device tests at incoming inspection were described, as well as how environmental stress screening and testing would be used in circuit-pack test, cable test, equipment test, and system test. In February 1994, the test plan was re-issued for a second time to incorporate the role of failure mode analysis (FMA) and to update the stressing practices.

The team, in conjunction with the customer, ruled on all issues relating to product reliability and testing. The group met monthly throughout product introduction and well into production, and played a major role in ensuring a consistent, high-quality product.

Environmental Stress Screening/Testing. Environmental stress screening/testing is a process in which environmental forces are applied to a product to drive latent or marginal defects into hard failures. The stress levels must be stringent enough to precipitate product weaknesses, yet not damage good product. Instituting ESS/T as part of the factory test regimen allows the early detection of infant mortality failures prior to product shipment to the field. The use of ESS/T in the 1B24 project had a two-fold purpose: guaranteeing design robustness and ensuring reliability in every shipped product.

Every production Fastech* circuit pack, as well as every ribbon cable, underwent 20 cycles of unbiased thermal stress from -20° centigrade (C) to 80° C at a

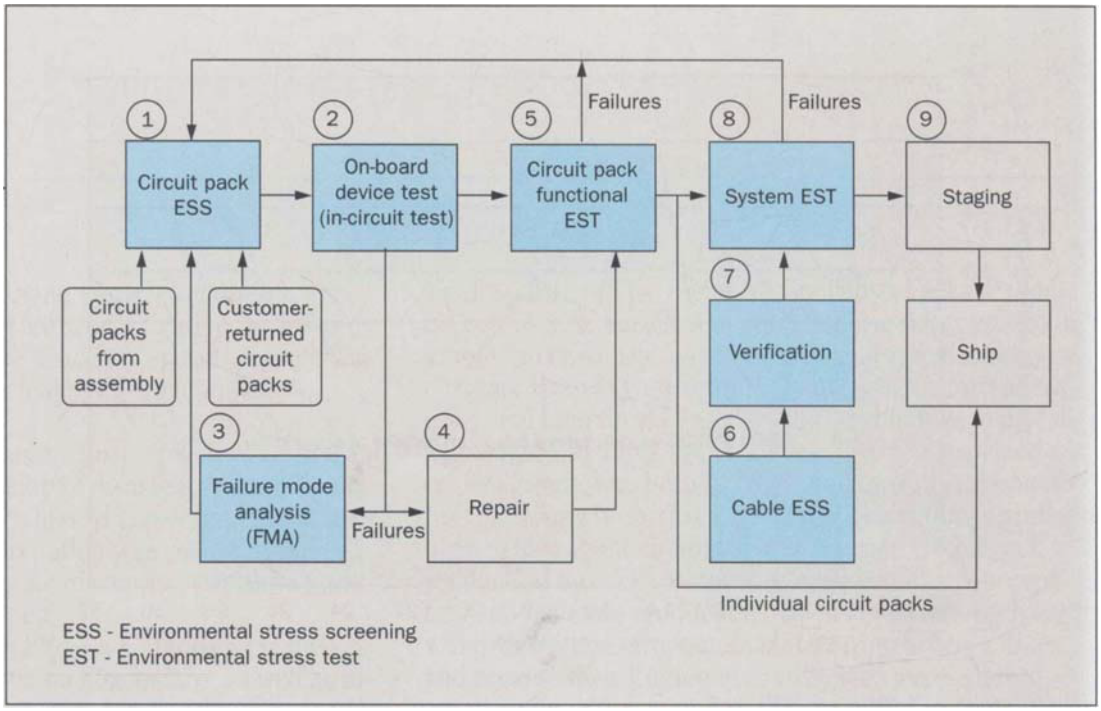

Figure 3. The production flow for product stress screening and testing (ESS/T) is shown here. Stress screening/testing was performed at four points in the manufacturing flow: cable ESS, circuit-pack ESS, circuit-pack functional EST, and EST at the system level.

ramp rate of 20° C per minute. Each of these circuit packs also was verified to operate via circuit-pack functional test (CPFT) system diagnostics at 80° C, 60, 0, -20, and 50, as well as room temperature.

The stressing profiles were derived from a multitude of ESS/T trials to ensure that the optimal profile for the product was used. During the preproduction phase of the project, every frame, cable, and circuit pack—except some select fuse cards—underwent the 20-cycle test profile. In addition, each pack was functionally tested at nine non-linear temperature steps: 30° C, 80, 60, 40, 20, 0, -20, 80, and 30.

All preproduction completed processors, having gone through all standard factory tests, were placed into a walk-in stress chamber and stressed during diagnostic phases run at the same nine-step temperature profile. This functional system test-environmental stress test (FSTEST) was performed on five preproduction processors, after which several systems went through a STRIFE (stress to life) test performed by design.

The first six production processors also underwent FSTEST to verify the integrity of the planned standard manufacturing processes, which do not include FSTEST. Failures, also called dropouts, at FSTEST due to the additional stressing were minimal. Some dropout, due to software and handling problems, was experienced and corrected. FSTEST results validated to the customer that the standard factory tests and stressing regimens sufficiently weeded out infant mortality failures.

The preproduction regimen of stressing all processor cables was altered to consist of ribbon cable stress only. During preproduction, 15 cable failures were detected among the 5,903 cables stressed—with all failures occurring on ribbon cables. The results of failure mode analysis led to a redesign of the connector, and it was decided to continue stressing the ribbon cables throughout the project rollout.

During preproduction, assembled frames—without circuit packs—were also stressed. No stress-related failures were uncovered other than the ribbon cable problems. Vibration of the frames was investigated and was found to be a problem, due to the design of the backplane assembly unit. Stressing of the frames ended in October 1993. The data collected at that time no longer supported continued frame thermal stress. The resultant production ESS/T product flow is shown in Figure 3.

The 20 cycles of circuit-pack ESS was maintained and the CPFT test profile consisted of six steps, as opposed to the nine steps used during preproduction. FSTEST was performed at 50° C and room temperature only. A number of correctable problems were uncovered through the implementation of ESS and CPFT EST on the 1B24 circuit packs throughout both the preproduction and production phases.

During preproduction, several temperature-dependent failures were found at CPFT. At first, the system would not operate much below room temperature, due to device programming race conditions. Emitter coupled logic reference voltage threshold problems also were discovered and corrected. A number of programmable logic devices (PLDs) also underwent reprogramming due to temperature-dependent timing problems. Some temperature and CPFT test-pad-dependent noise problems were detected and corrected through circuit-pack

redesign. Many performance margins were improved directly or indirectly.

The commitment of the design team to correct temperature-related design issues was essential to any ESS/T strategy and product performance prediction. Without the responsiveness of the design team in addressing these issues, the factory ESS/T regimen never would have been able to contribute as much as it has to this project.

Unlike design issues brought out during the early implementation of ESS/T, component issues were dealt with on an ongoing basis. Circuit-pack ESS propagated numerous problems in vendor components before they made their way to the field. In two such cases, we approached the vendor with our results and were jointly investigating the problem when other customers of the vendor alerted the vendor to the same problem—only in their case, the problem was being found in the field.

Manufacturability Audit. At the completion of the preproduction phase, executive management and the 1B management team felt it necessary to conduct an independent manufacturability audit. A very detailed set of reviews was conducted by an independent audit team, including the customer, design, manufacturing, and deployment. The results were reported to the team and executive management. The project "passed" the audit.

Further, the audit confirmed current plans and actions, uncovered additional areas for further assurance or contingency planning and, equally important, helped further enhance the cohesiveness of the project team.

As it is not necessarily the norm in our culture to view audits as positive events, everyone was assured in advance that this audit was to improve future efforts, and not to find past faults. Based on our positive experience, we encourage other organizations to use audits to enhance the knowledge of a project, as well as to enhance team building.

Change Management. The project was managed through an elaborate time table that included all associated functional AT&T organizations. Processor delivery, installation schedules, and retrofit dates were all documented and disseminated throughout the appropriate organizations. The goal of the change management team was to incorporate as many design and quality enhancements into both the preconditioning and main material deliverables without missing any of the established dates.

To accomplish these objectives, the project put "communication" into overdrive: daily cross-functional manufacturing meetings, weekly design coordination meetings, and weekly corporate product realization group (CPRP) deployment meetings. A variety of media were used to consolidate, display, and report the necessary data about change orders and the resulting circuit-pack configuration by machine.

Through these efforts, Class A change cycle time reduction improvements were accomplished. In November 1992, it took 70 days to process Class A circuit-pack changes. By January 1994, this interval took as little as four days. The team processed over 66 Class A changes on circuit packs, over 150 cable changes, and numerous equipment changes.

Facilities and Processes. In this section, we discuss circuit-pack functional tests, bonepile recovery, in-circuit testing, firmware, and failure mode analysis.

Circuit-Pack Functional Test. The objective of the 1B circuit-pack functional test was to provide reliable field-grade circuit packs for either direct shipment to the field or to factory system test for testing with a completed frame. The CPFT strategy was to test circuit packs using the same generic software that is run in AT&T's 4ESS network. Although the generic software contains elements that are undesirable in a testing environment, the advantages are that both software and hardware problems are discovered before they reach the field. This requires a significant amount of 4ESS peripheral equipment, including two attached processor interface units, two data unit selector units, an input/output processor, and a peripheral unit bus branching frame to support each CPFT test pad.

In addition, each test pad consists of a thermally enclosed 1B processor frame that is known to be good, or "golden," with a complete set of golden circuit packs, a 3B20 minicomputer on which the 1B generic resides and from which the 1B boots, a Sun workstation for testing the 1B utility system, a maintenance control console terminal, and a maintenance teletype terminal, exactly as it would appear in the field.

CPFT EST consists of functionally testing the circuit packs while varying the temperature, as previously noted, between 80° C and -20° C (see Figure 4). The testing includes not only diagnostics, but the additional

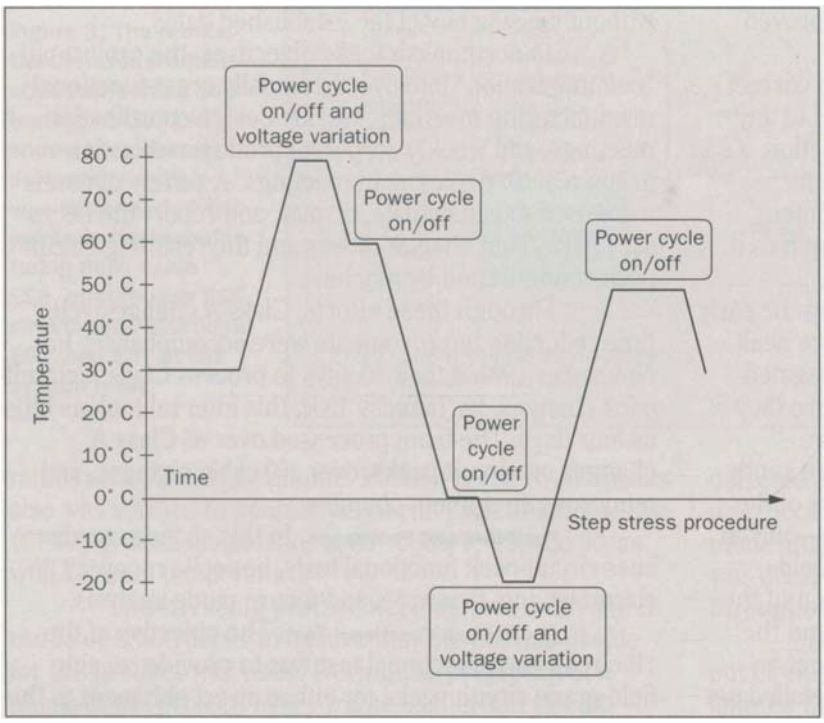

Figure 4. Circuit-pack functional test/environmental stress test (CPFT EST) consists of functionally testing the circuit packs while varying the temperature, in this case between 80° centigrade (C) and -20° C. The testing includes not only diagnostics, but the additional stress factors of power cycling and input voltage variations at the two extreme temperatures.

stress factors of power cycling and input voltage variations at the two extreme temperatures. At each intermediate step, a complete set of diagnostics and power cycling is performed. The circuit packs endure a last step at 50° C where special functional tests are run, in addition to a complete set of diagnostics. The special functional tests check any circuitry that is untested by diagnostics.

Early on, the challenge was to determine the correct number of CPFT pads to accommodate the schedule. Estimating a two-shift operation of 25 packs (roughly one quarter of a system) per CPFT cycle at eight hours per cycle, simulation determined that four pads were necessary to handle the peak load. However, as the test requirements became clearer and as diagnostic coverage and length increased, so did the cycle time. In March 1993, the average CPFT test cycle took 58 hours. In an effort to shorten the run times of the longest diagnostics, quality process management was invoked by the test engineering team and the software developers. Targeted test phases were analyzed and portions rewritten. Diagnostics that took over five hours to run are now executed in less than 40 minutes.

Based on an analysis of the CPFT failure data and a re-examination of the EST objectives, the ITP team determined that certain temperature steps could be combined into a much more compact test profile and still realize the same quality. These alterations resulted in a 3- to 4-hour improvement in cycle time.

To further improve the situation, heavy emphasis was placed on engineering shop support and continuous tester training. A special training class had been developed for the testers and engineers and was delivered by the AT&T Training Center in Dublin, Ohio. Following the class, weekly tester and engineering meetings were held to discuss problems and solutions. The key was providing immediate feedback and answers to issues raised by the testers during these meetings. As a result, measurable improvements were made in both cycle time and in the number of circuit packs tested per cycle.

The most difficult part of CPFT, however, was determining the proper tests to run. Each circuit pack has its own test requirements, some of them overlapping. Some even offer a choice. The most efficient set of diagnostics and tests was not always being run, resulting in increased cycle time. To combat this, the automated test process program was developed. The program guides the tester through an entire cycle by automatically changing the temperature, varying the voltage, and power cycling the circuit packs under test at the proper time.

The most efficient set of diagnostics is run at each step, based on the circuit packs being tested, and defect data is collected automatically. The collective result of all of these cycle-time improvements was a 19-hour average cycle time by June of 1994—a 67 percent reduction. Without this work, the factory would have needed

triple the number of planned CPFT facilities at an additional cost of $10 million.

Bonepile Recovery. One of the five CPFT pads was primarily used for engineering troubleshooting. Bonepile packs—packs that passed in-circuit testing but still wound up on the "bone pile" because they failed CPFT—were investigated on this facility. Engineers and designers worked aggressively to correct these difficult functional failures as part of the project plan. Due to the quick project rollout and the finite amount of processors needed, bonepile issues had to be addressed quickly or there would be no substantial need for any of these repaired—and totally usable—boards at later dates. To date, $1.65 million has been recovered and only 0.25 percent of the production packs had to be scrapped.

In-Circuit Test (ICT). Typically, in-circuit tests are developed and verified using a circuit pack that has passed all tests at the system level. It is not until sufficient quantities of circuit packs have been produced, and in many cases deployed, that shortcomings in the assembly process, the reliability of the components, or the stability of the ICT itself are discovered.

The 1B ICT engineering team explored and implemented non-traditional and proactive measures during the preproduction phase of the project. Key activities included:

- Employing full-cell memory tests,
- Terminating inputs to differential devices and floating CMOS inputs at the edge connectors,
- A disciplined indicted (suspected failures) parts analysis process,
- Development of a suite of utilities designed to assist the test operators in troubleshooting, and
- Board-level physical fault insertion, called board grading.

Board grading is a HP3070 software utility that thoroughly inspects the quality, reliability, repeatability, and comprehensiveness of an in-circuit test. The utility tests and verifies various aspects or features of the in-circuit test. Physical fault insertion, perhaps the most fundamental stage of board grading, is a process that measures the in-circuit test's ability to detect assembly errors and defective components. Fault insertion provides a detailed analysis of how complete and comprehensive the in-circuit tests are. This information can then be used for test improvement.

All 35 of the 1B in-circuit tests were subjected to this analysis over a six-month period. Through these efforts, an average of 99.2 percent pin fault coverage was achieved across all codes. During this period, the ICT's downstream customer, CPFT, experienced a 15% increase in first-pass yields (refer to Figure 5). At an average of 120 hours per code to run, analyze, and upgrade the tests, it is obvious how resource-intensive this board grading was. However, the estimated $1.55 million savings due to reduction in CPFT troubleshooting effort overshadowed the associated costs.

Many of the improvements that were implemented would not have been possible without the cooperation of design engineering. Had the devices not been testable as designed, the improvement opportunities identified through board grading would have been, for the most part, unattainable.

Firmware. The 1B24 processor uses a high concentration of programmable logic devices. In fact, 3,120 programmable devices exist in a processor, with 179 present on one circuit-pack code alone. It was especially important to ensure the highest programming quality possible. Detecting programming mistakes prior to board insertion reduces rework that adversely effects both cost and quality. To meet these objectives, the group concentrated on increased vector testing, parametric testing, process improvements, and automation.

The ITP test plan targeted all unique PLD test programs for 95 percent or greater fault coverage for logic and intact fuses. Test and design worked diligently to attain this level, and only seven PLD programs of more than a thousand fell short of this ambitious goal.

Parametric testing was a major part of the firmware strategy. Although a part with parametric failures will often perform correctly today, it could fail a week, a month, or a year later, which was not acceptable. Therefore, the Logue McDonald 324b parametric tester was selected to test parts during the programming stage. The Logue system is connected directly to the programmer and handler so that the system is what is called "tube-to-tube," with programming, testing, and labeling in one step. With this one-step ability and the high integrity of the tests, process checking was not needed.

Issue control and specific device programs were managed via the Focus Prime design transfer tool, an AT&T tool that provides an integrated software environ-

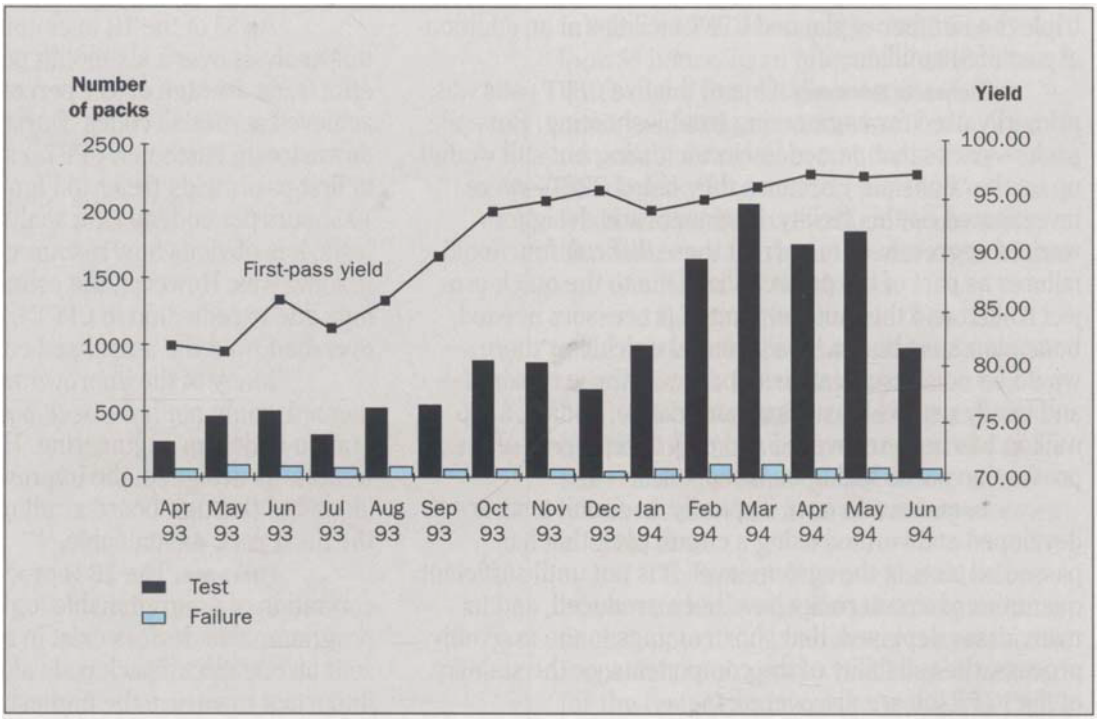

Figure 5. All 35 of the 1B in-circuit tests were subjected to board grading analysis over a six-month period. Through these efforts, an average of 99.2 percent pin fault coverage was achieved across all codes. During this period, the ICT's downstream customer, circuit-pack functional test (CPFT), also experienced a 15% increase in first-pass yields.

ment, and a personal computer network interface linked directly to device programmers

Failure Mode Analysis (FMA). The goal of failure mode analysis is to provide timely, simplistic, and technically sound feedback to the designers, process engineers, product engineers, and suppliers so that a defect can be quickly analyzed and prevented from reoccurring. 1B24 FMA was driven by four strategies:

- Stringent customer reliability requirements,
- Prompt investigation of all problems found during EST, manufacturing, and from field returns,
- Advance warning of parts or processes going out of control, and
- Assisting suppliers in providing reliable parts.

A simple but effective method of tracking and controlling defective components was put into place. Once defective components are removed from a circuit pack, tracking is accomplished by assigning a unique number to each indicted part via a pre-numbered bag. This number is then entered into the ICT defect data-collection database, associating it with the appropriate failure. The number is used when corresponding with FMA facilities both inside and outside AT&T, resulting in less confusion when multiple examples of similar defects are being discussed. A history of each pack by type and serial number, and the number and type of any defects that have occurred, can also be easily generated from this database.

Support for the 1B FMA effort has come from several sources, including the vendors whom we rely on for root cause analysis of defects in components they supply. Resources inside AT&T also have been frequently used when a vendor is unable to perform a satisfactory defect analysis. The AT&T Global Supply Line Management's (GLSM's) Centers of Excellence for both integrated circuits and passive components have been used extensively on this project to perform both root-cause analysis and to serve as consultants to the 1B team. The GSLM expertise, coupled with the excellent work performed in the FMA lab in Columbus, resulted in some tremendous work benefiting not only those on the project, but the associated outside vendors as well.

Processes

In this section, we discuss the steps taken to optimize four key processes in the manufacturing project.

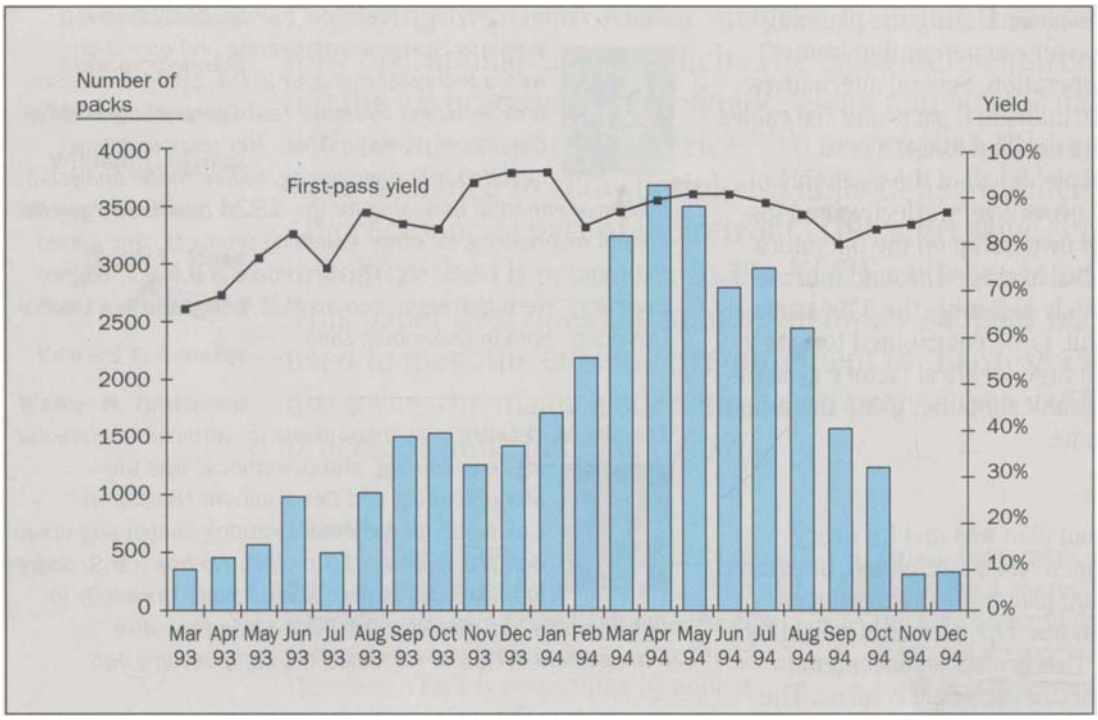

Figure 6. Automated visual inspection technology, in which a machine makes a "visual" check for bent pins and misinsertions before soldering, resulted in product being 99.98 percent accurate with respect to pin defects. In-circuit testing (ICT) first-pass production yields are shown in this figure.

Wave-Solder Process. Most 1B processor circuit packs were the large size (13 by 16 inches) KLW boards averaging 825 components—entirely through-hole—and 5,345 solder joints per board. Over the course of the production phase of the 1B processor, the wave-solder quality was improved from 384 defects per million solder joints in production to 23 defects per million. The quality improvement record is attributed to:

- Developing special fixtures to minimize board warping and bowing and to minimize the need for solder touch-up activities,
- Finding optimum soldering parameters for various codes,
- Establishing a comprehensive preventive maintenance plan for the equipment, and
- Having a well-trained and quality conscious manufacturing team.

Circuit-Pack Assembly. The objective of the 1B manufacturing process was to build quality into the product through simple processes and continuous improvements, *not* through inspection. No process checking was used. Instead, an independent organization each day performed quality sample monitoring, and the results were reported in the Columbus Quality Information System. This data was reviewed by the cell teams of individual operations on a weekly basis, or as necessary.

Critical to the assembly of large, dense circuit packs was automated visual inspection technology, in which a machine makes a "visual" check for bent pins and misinsertions before soldering. The data from the vision machine proved very valuable in identifying root causes and making improvements. It also allowed production associates to correct all defects found at vision, which resulted in product continuing on to future operations being 99.98 percent accurate with respect to pin defects. ICT first-pass production yields are shown in Figure 6

Cables. The cable fabrication operation was more complex than usual, due to the numbers of cables required for both conversion-switch and processor ships. Also, this was the first time ship kitting—kits of about 500 cables organized for installers—was integrated into the cable assembly shop, making it unique among cable operations. Although initially difficult from the perspective of documentation and execution, this proved to be both necessary and successful.

Equipment Team Building. During the planning phase of the project, it became apparent that frame assembly was a critical operation. Several alternatives for assembling over 9,000 individual parts and 700 cables were reviewed, and it was decided to use a craft approach, where two people did all of the assembly of one frame. This method proved very effective and fostered an intense sense of ownership on the operators' part. The assembly interval averaged around four weeks for two people to completely assemble the 9,700 parts and cables. The ownership issue contributed to a very high level of quality, with high yields at factory systems test and a minimum of troubleshooting, given the inherent complexity of the frame.

Summary

The project rollout plan was met for every required processor shipment via a disciplined, integrated, and audited manufacturing plan mutually developed across multiple organizations. The pursuit of reliability on this product paid off. This project achievement is apparent in the data on circuit-pack field returns. The current field dropout rate is 0.05 packs/system/week, which is better than the project requirement of 0.50 packs/system/week by a factor of 10. It also surpasses the current 1A processor dropout rate by a factor of two. To be able to surpass—from the outset—the reliability of a stable product is an exceptional accomplishment.

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Trademarks

* Fastech is a trademark of Berg Electronics Inc.

***Lisa A. Flynn**, currently a technical manager in Network Wireless Systems engineering and operations, was a technical manager in the 1B24 Processor and Switching Systems Test Group at the AT&T Columbus Works in Ohio. Her responsibilities included test engineering, failure mode analysis, and environmental stressing for the 1B24 processor, as well as test engineering for other switching products. She joined the company in 1985. Ms. Flynn received a B.S.E.E. degree from Ohio State University and an M.B.A. degree from Capital University, both in Columbus, Ohio.*

***Thomas M. O'Leary**, now responsible for wireless manufacturing, engineering, and operations, was the Manufacturing and Development Director at Columbus for the manufacturing design and operation phase of the 1B project. He has a B.S. degree in mathematics from Illinois State University in Chicago, and has attended the Penn State Executive Management Program. He joined the company in 1965.*