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# Computing Inductive Noise of Chip Packages

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Inductive noise limits the physical design of high-speed, high pin-out chip packages. This paper presents the derivation of some basic equations that are useful for computing inductive noise of various chip packages, and also presents simple asymptotic and limiting results that reduce to some useful approximate results proposed by others. These results are helpful for computing inductive noise in arrays of wire bonds, solder balls, dual in-line package leads, package pins, and connector pins. Computed results agreed well with measured results. We present two simple rules for minimizing inductive noise and also discuss the inductive noise of power and ground planes.

## I. INTRODUCTION

If $n$ drivers each switch current at $\dot{I} = 20$ mA/ns, the inductive noise across a common ground lead inductance, $L_g$, is approximately $nL_g\dot{I}$. For a 32-bit processor and $L_g = 1$ nh, this inductive noise component is about (32)(1 nh) 20mA/ns = 640 mV. It is known that a 50-mil-long wire bond used as an input/output (I/O) lead of an integrated circuit chip has a self-inductance of about 1 nh. Thus, many such leads must be connected in parallel to reduce this inductive noise component to tolerable levels. This is necessary because present large-scale integrated (LSI) circuits have a total noise margin of only a few hundred millivolts. This inductive noise problem has been recognized and discussed by C. W. Deisch.[1]

This paper derives some general equations that are useful for computing the inductive noise of high-speed, high pin-out chip packages.

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A basic role is played by the mutual inductance between two parallel conductors.

## II. MUTUAL INDUCTANCE OF TWO PARALLEL CONDUCTORS

Consider the two parallel conductors shown in Fig. 1. By applying the Biot-Savart law,[2] a current $I$ flowing in the $y$ direction produces a magnetic flux density, $B(x, y)$, given by

$$B(x, y) = \frac{\mu I}{4\pi} \int_{-\ell/2}^{\ell/2} \frac{\sin \theta}{r^2} dy_0 = \frac{\mu I}{4\pi} \int_{-\ell/2}^{\ell/2} \frac{x}{r^3} dy_0 \tag{1}$$

$$= \frac{\mu I}{4\pi x} \left[ \frac{(y + \ell/2)}{\sqrt{(y + \ell/2)^2 + x^2}} - \frac{(y - \ell/2)}{\sqrt{(y - \ell/2)^2 + x^2}} \right], \tag{2}$$

where $\mu$ = permeability of the medium. The total flux, $\Lambda$, linking the idle conductor is then given by

$$\Lambda \equiv \int_d^\infty dx \int_{-\ell/2}^{\ell/2} B(x, y) dy$$

$$= \frac{\mu I \ell}{2\pi} \left[ ln \left( \frac{\ell}{d} + \sqrt{1 + \left(\frac{\ell}{d}\right)^2} \right) - \sqrt{1 + \left(\frac{d}{\ell}\right)^2} + \frac{d}{\ell} \right]. \tag{3}$$

If the medium is a vacuum or air, then $\mu = \mu_0 = (4\pi)10^{-7}$ h/m and the mutual inductance, $M$, is given by

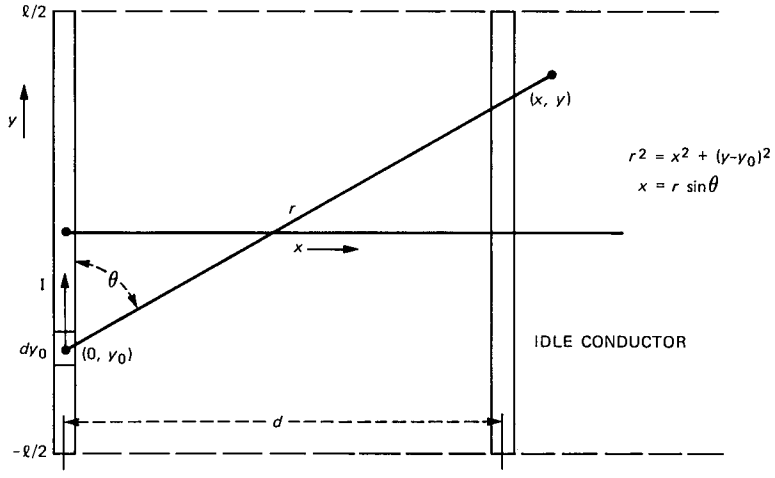


Fig. 1—Coordinate system for derivation of mutual inductance.

$$M \equiv \frac{\Lambda}{I} \doteq 5\ell \left[ \ln\left( \frac{\ell}{d} + \sqrt{1 + \left(\frac{\ell}{d}\right)^2} \right) - \sqrt{1 + \left(\frac{d}{\ell}\right)^2} + \frac{d}{\ell} \right] \text{nh}, \quad (4)$$

where

$\mu_0/2\pi \doteq 5$ nh/in

$\ell$ = length in inches

$d$ = separation in inches.

A useful asymptotic result for small $d/\ell$ is given by

$$M \sim 5\ell \left[ \ln\left(\frac{2\ell}{d}\right) - 1 + \frac{d}{\ell} - \left(\frac{d}{2\ell}\right)^2 \right] \text{nh}. \quad (5)$$

Equation (4) can also be derived by evaluating the Neumann inductance integral. Equations (4) and (5) agree with eqs. (1) and (3) of Ref. 3.

The inductances discussed in this paper are more precisely known as partial self and mutual inductances. However, we shall follow Ref. 3 and refer to them as merely self and mutual inductances.

## III. SELF-INDUCTANCE OF A STRAIGHT CONDUCTOR

### *3.1 Self-inductance resulting from the internal field*

Consider the current element shown in Fig. 2. A basic definition of self-inductance, $L$, is

$$L \equiv \frac{N\phi}{I} = \text{total number of flux linkage per ampere.} \quad (6)$$

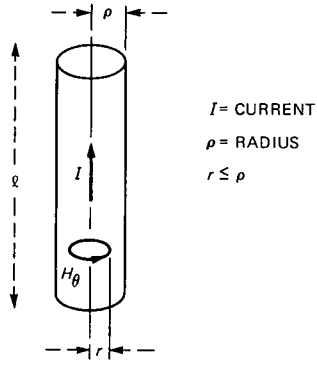


Fig. 2—Notation for derivation of self-inductance.

From Maxwell's equation[2] (i.e., Ampere's law), the magnetic intensity, $H_\theta$, internal to the conductor is given by

$$\oint \vec{H} \cdot \vec{ds} = \left(\frac{I}{\pi\rho^2}\right)(\pi r^2) = I\left(\frac{r}{\rho}\right)^2 \qquad 0 \le r \le \rho. \tag{7}$$

Equation (7) assumes that the current density, $I/(\pi\rho^2)$, is uniform in the conductor. (Skin effect is neglected. References 2, 3, and 4 show that skin effect tends to reduce the internal self-inductance, $L_i$.) From eq. (7),

$$H_\theta \equiv |\vec{H}| = \frac{I}{2\pi r}\left(\frac{r}{\rho}\right)^2 \qquad 0 \le r \le \rho. \tag{8}$$

The flux density, $B_\theta$, internal to the conductor is then

$$B_\theta \equiv \mu H_\theta = \frac{\mu I}{2\pi r}\left(\frac{r}{\rho}\right)^2 \qquad 0 \le r \le \rho. \tag{9}$$

As Ref. 4 shows, a given flux line of radius $r \le \rho$ encloses a fraction $(r/\rho)^2$ of the total current $I$. Thus, from eqs. (6) and (9) the self-inductance, $L_i$, resulting from the internal magnetic field is

$$L_i = \frac{\ell}{I}\int_0^\rho B_\theta \left(\frac{r}{\rho}\right)^2 dr = \frac{\mu\ell}{8\pi}. \tag{10}$$

Equation (10) can also be derived from internal energy considerations. If $\mu = \mu_0$, and $\ell$ is in inches,

$$L_i = \left(\frac{\mu_0}{2\pi}\right)\left(\frac{\ell}{4}\right) \doteq 5\left(\frac{\ell}{4}\right) \text{ nh.} \tag{11}$$

### *3.2 Total self-inductance*

The total self-inductance, $L_s$, of a straight conductor is obtained by adding the contributions from the external and internal magnetic fields. Thus, from eqs. (4) and (11) we have

$$L_s = M|_{d=\rho} + L_i = M|_{d=\rho} + 5\left(\frac{\ell}{4}\right) \text{ nh.} \tag{12}$$

Also, for small $\rho/\ell$,

$$L_s \sim 5\ell\left[ln\left(\frac{2\ell}{\rho}\right) - \frac{3}{4}\right] \text{ nh.} \tag{13}$$

Equation (13) agrees with eq. (7) of Ref. 3.

When the cross section of the conductor is rectangular, Ref. 3 shows that the self-inductance is given by

$$L_s \doteq 5\ell \left[ \ln\left(\frac{4\ell}{p}\right) + \frac{1}{2} \right] \text{nh}, \tag{14}$$

where $p$ = perimeter of cross section in inches.

## IV. INDUCTANCE OF POWER AND GROUND PLANES

Consider the power and ground (P/G) planes shown in Fig. 3. Assume that both planes carry equal, thin sheets of current, $I$, in opposite directions. Again, using Ampere's law,

$$\oint \vec{H} \cdot \vec{ds} = I. \tag{15}$$

The magnetic field is more intense and approximately uniform in the space between the P/G planes. The magnetic field outside the planes is assumed to be negligible because of field cancellation. Thus,

$$|\vec{H}|\, W \equiv HW = I, \tag{16}$$

$$B \equiv \mu H = \frac{\mu I}{W}, \tag{17}$$

and

$$L \equiv \frac{N\phi}{I} = \frac{B\ell h}{I} = \frac{\mu \ell h}{W}. \tag{18}$$

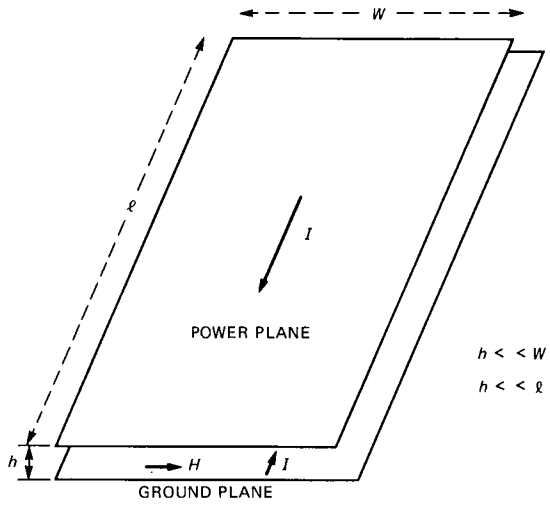


Fig. 3—Notation for derivation of inductance of P/G planes.

If $\mu = \mu_0$, and $\ell$ is in inches,

$$L = \left(\frac{\mu_0}{2\pi}\right) 2\pi\ell \left(\frac{h}{W}\right) = 10\pi\ell \left(\frac{h}{W}\right) \text{ nh.} \tag{19}$$

One half of this $L$ is associated with the ground plane and the other half is associated with the power plane. Thus, the inductance of the ground plane, $L_g$, and the inductance of the power plane, $L_p$, are given by

$$L_g = L_p = 5\pi\ell\left(\frac{h}{W}\right) \text{ nh.} \tag{20}$$

## V. COMPUTING INDUCTIVE NOISE

### *5.1 Pair of conductors*

Consider the pair of conductors shown in Fig. 4. The noise voltage, $v_n$, is a result of the self and mutual inductances of the conductors. Thus, using eqs. (12) and (4),

$$v_n = L_s\dot{I} - M\dot{I} = (L_s - M)\dot{I} \text{ mV,} \tag{21}$$

where $\dot{I} = dI/dt$ = time rate of change of current, mA/ns.

For small $d/\ell$, eqs. (5), (13), and (21) yield the asymptotic result

$$v_n \sim 5\ell\dot{I}\left[\ln\left(\frac{d}{\rho}\right) + \frac{1}{4} - \left(\frac{d}{\ell}\right) + \left(\frac{d}{2\ell}\right)^2\right] \text{mV,} \tag{22}$$

where $\ell$, $d$, $\rho$ are expressed in inches and $\dot{I}$ is expressed in mA/ns. As $d/\ell \to 0$, eq. (22) agrees with eq. (6-26) of Ref. 4 and eq. (16) of Ref. 3. Also, the first term of eq. (22), or

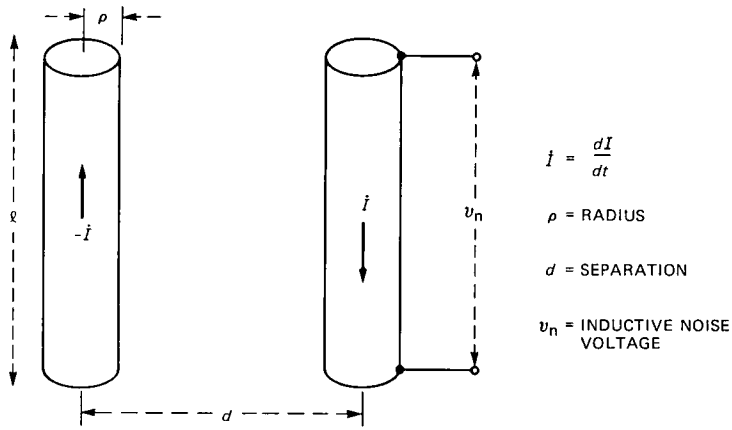


Fig. 4—Notation for derivation of inductive noise voltage, $v_n$.

$$v_n \doteq 5\ell\dot{I}\ln\left(\frac{d}{\rho}\right) \text{ mV} \tag{23}$$

was proposed as an approximation in the work reported in Ref. 1.

Table I shows some numerical values of inductive noise voltages for a pair of conductors such that $\dot{I} = 20$ mA/ns, $\ell = 0.2$ inches, $\rho = 0.01$ inches, and $d = 0.1$, 0.2, 0.3, and 1.0 inch. These numerical results show that the "exact" inductive noise voltage is somewhat less than that given by the approximate eq. (23). However, for small $d/\ell$, the results obtained from eqs. (23) or (22) are suitable.

In general, the duration of the inductive noise voltages is approximately equal to the signal rise time.

### *5.2 Array of conductors*

#### *5.2.1 General equations*

Consider an array of $N + 1$ conductors having equal lengths, $\ell$, equal radii, $\rho$, and separations, $d_i$, as shown in Fig. 5. Let us compute the inductive noise voltage, $v_n$, induced in a particular conductor located

Table I—Inductive noise voltages for a pair of conductors

| $d$ | $d/\dot{I}$ | $\dot{I} = 0.2$ in., Approximate (eq. 23) | $\rho = 0.01$ in., Exact (eq. 21) | $\dot{I} = 20$ mA/ns, Asymptotic (eq. 22) |
|---|---|---|---|---|
| 0.1 in. | 0.5 | 46.0 mV | 43.25 mV | 42.3 mV |
| 0.2 | 1.0 | 60.0 | 50.4 | 49.9 |
| 0.3 | 1.5 | 68.0 | 53.3 | 54.3 |
| 1.0 | 5 | 92.1 | 57.8 | 122.1 |

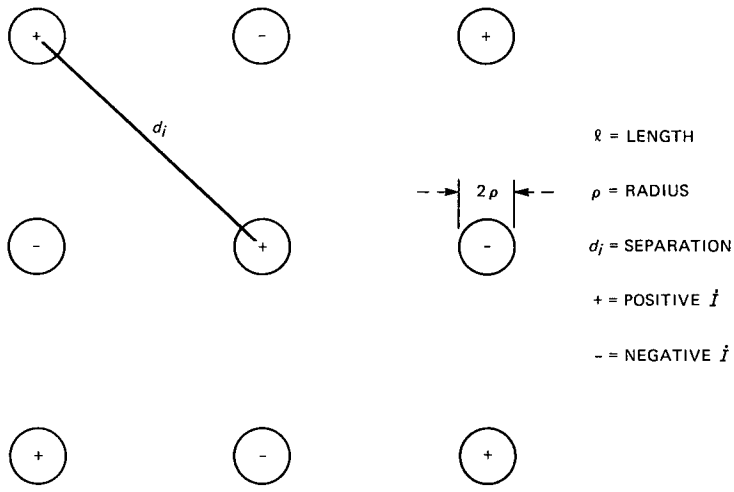


Fig. 5—Array of conductors.

at the center for convenience. Let us denote the rate of current change by $\dot{I}_i$(mA/ns), where $i = 0, \cdots, N$ with $i = 0$ denoting the particular conductor of interest.

One component of the inductive noise voltage, $v_m$, is a result of the mutual inductances (i.e., inductive crosstalk) and is given by

$$v_m = \sum_{i=1}^{N} M_i \dot{I}_i \text{ mV}, \tag{24}$$

where $M_i$ is given by eq. (4) with

$$M_i \equiv M|_{d=d_i}.$$

The other component of the inductive noise voltage, $v_s$, is a result of the self-inductance of the particular conductor and is given by

$$v_s = L_s \dot{I}_0 \text{ mV}, \tag{25}$$

where $L_s$ is given by eq. (12). Thus, the total inductive noise voltage, $v_n$, induced in the particular conductor is given by

$$v_n = v_s + v_m = L_s \dot{I}_0 + \sum_{i=1}^{N} M_i \dot{I}_i \text{ mV}. \tag{26}$$

Equation (26) is the most general equation for computing the inductive noise of an array of conductors.

If the $\dot{I}_i$ in the array of conductors are constrained so that they satisfy the subsidiary condition (i.e., Kirchhoff's current law),

$$\sum_{i=0}^{N} \dot{I}_i = 0, \tag{27}$$

then eq. (26) can be written as

$$v_n = -\sum_{i=1}^{N} (L_s - M_i)\dot{I}_i \text{ mV}. \tag{28}$$

This equation is a generalization of eq. (21). Also, if eq. (27) holds, then for small $d_i/\ell$, eqs. (5), (13), and (26) yield the asymptotic result

$$v_n \sim 5\ell \left\{ -\dot{I}_0 \left( \ln(\rho) - \frac{1}{4} \right) - \sum_{i=1}^{N} \dot{I}_i \left[ \ln(d_i) - \left( \frac{d_i}{\ell} \right) + \left( \frac{d_i}{2\ell} \right)^2 \right] \right\} \text{ mV}, \tag{29}$$

where $\ell$, $d_i$, $\rho$ are expressed in inches and the $\dot{I}$'s are expressed in mA/ns.

If all $d_i/\ell \to 0$, eq. (29) reduces to eq. (6-27) in Ref. 4. If all $d_i/\ell \to 0$, and $|\ln(\rho)| \gg 1/4$, eq. (29) reduces to eq. (2) of Ref. 1,

namely,

$$v_n \doteq 5\ell \left\{ -\dot{I}_0 \ln(\rho) - \sum_{i=1}^{N} \dot{I}_i \ln(d_i) \right\} \text{ mV}. \tag{30}$$

If all conductor separations $d_i \to \infty$, only the self-inductance of the conductor introduces inductive noise and eq. (26) reduces to

$$v_n = L_s \dot{I}_0. \tag{31}$$

In contrast, eqs. (29) and (30) are not applicable if any of the $d_i \to \infty$.

### *5.2.2 Grounded wire bonds*

As an example of computing inductive noise voltage across common ground leads in an array of conductors, consider the particular array of signal, power, and ground wire bonds on an integrated circuit chip shown in Fig. 6. Let us suppose each of the 32 signal bits switch current, simultaneously, at a rate of $\dot{I}$ mA/ns through the signal (S) wire bonds, as indicated in Fig. 6. What is the induced noise voltage, $v_n$, across the common ground (G) leads? We shall assume that when the G leads switch, the P leads are idle. This is a property shared by many chip driver circuits. We shall also assume that the magnetic fields associated with wire bonds on different sides of the chip do not interact significantly. Finally, the chip driver circuits are assumed to be, approximately, uniformly loaded.

From Kirchhoff's current law,

$$2\dot{I}_1 + \dot{I}_2 + 8\dot{I} = 0. \tag{32}$$

From eq. (26), the voltage $v_1$, at the corner grounds is

$$v_1 = L_s \dot{I}_1 + \dot{I} m_1 + \dot{I} m_2 + \dot{I}_2 M_{10\Delta} + \dot{I}_1 M_{20\Delta}, \tag{33}$$

where $L_s$ is given by eq. (12),

$$m_1 = M_{2\Delta} + M_{3\Delta} + M_{7\Delta} + M_{8\Delta}$$

$$m_2 = M_{12\Delta} + M_{13\Delta} + M_{17\Delta} + M_{18\Delta},$$

and $M_{i\Delta}$ is given by eq. (4) with

$$M_{i\Delta} \equiv M|_{d=i\Delta}.$$

Similarly, the voltage, $v_2$, at the center grounds is

$$v_2 = L_s \dot{I}_2 + 2\dot{I} m_1 + 2\dot{I}_1 M_{10\Delta}. \tag{34}$$

By equating $v_1 = v_2$, the common ground condition, and using eq. (32), there result two simultaneous equations:

$$A_1 \dot{I}_1 + B_1 \dot{I}_2 = C_1 \dot{I} \tag{35}$$

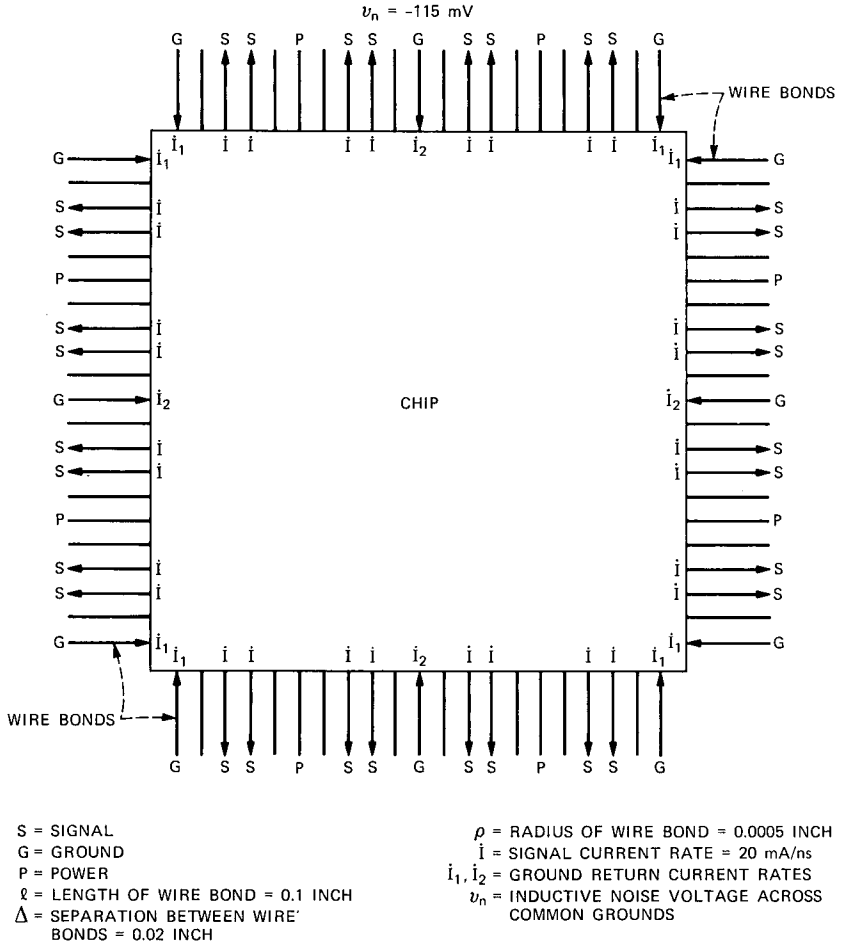


Fig. 6—Driver circuits on integrated circuit chip switching 32 signal bits simultaneously, with $v_n = -115$ mV.

$$2\dot{I}_1 + \dot{I}_2 = -8\dot{I}, \tag{36}$$

where

$$A_1 = L_s + M_{20\Delta} - 2M_{10\Delta}$$

$$B_1 = M_{10\Delta} - L_s$$

$$C_1 = m_1 - m_2.$$

The solution of eqs. (35) and (36) is

$$\frac{\dot{I}_1}{\dot{I}} = \frac{C_1 + 8B_1}{A_1 - 2B_1} \tag{37}$$

$$\frac{\dot{I}_2}{\dot{I}} = \frac{-2[4A_1 + C_1]}{A_1 - 2B_1}. \tag{38}$$

From eq. (34), the inductive noise voltage, $v_n$, across the grounded wire bonds becomes

$$v_n = v_2 = v_1 = \left[L_s\left(\frac{\dot{I}_2}{\dot{I}}\right) + 2m_1 + 2\left(\frac{\dot{I}_1}{\dot{I}}\right)M_{10\Delta}\right]\dot{I} \text{ mV}. \tag{39}$$

If $\ell = 0.1$ inch, $\Delta = 0.02$ inch, $\rho = 0.0005$ inch and $\dot{I} = 20$mA/ns, the results are

$$\begin{aligned} L_s &= 2.623 \text{ nh} \\ \dot{I}_1 &= -2.577\dot{I} \text{ mA/ns} \\ \dot{I}_2 &= -2.846\dot{I} \text{ mA/ns} \\ m_1 &= 1.1675 \text{ nh} \\ M_{10\Delta} &= 0.1226 \text{ nh} \\ v_n &= -115.2 \text{ mV}. \end{aligned} \tag{40}$$

As an approximation, one can assume a uniform distribution of return current rates and apply eq. (30). The results are

$$\begin{aligned} \dot{I}_1 = \dot{I}_2 &= -8\dot{I}/3 = -2.667\dot{I} \text{ mA/ns} \\ v_1 &= -122.9 \text{ mV} \\ v_2 &= -91.91 \text{ mV}. \end{aligned} \tag{41}$$

The average of $v_1$, $v_1$ and $v_2$ is $-112.57$ mV, which is approximately equal to $v_n$ of eq. (40). This averaging method was used in Ref. 1, and it can also be used with the exact eqs. (26) or (28) to obtain approximate results.

As a nonsymmetrical example, consider the particular array of wire bonds shown in Fig. 7. To simplify the analysis, we shall neglect the mutuals on the nonsignal sides of the chip. By eq. (27), we have

$$2[\dot{I}_3 + 2\dot{I}_1 + \dot{I}_2] + 32\dot{I} = 0. \tag{42}$$

Again, by using eqs. (26) one can write equations for $v_1$, the voltage across the corner grounds, $v_2$, the voltage across the center grounds, and

$$v_3 = L_s\left(\frac{\dot{I}_3}{3}\right). \tag{43}$$

By equating $v_1 = v_2 = v_3$, the common ground condition, and using eq. (42), there result three independent equations for $\dot{I}_1$, $\dot{I}_2$, and $\dot{I}_3$. By

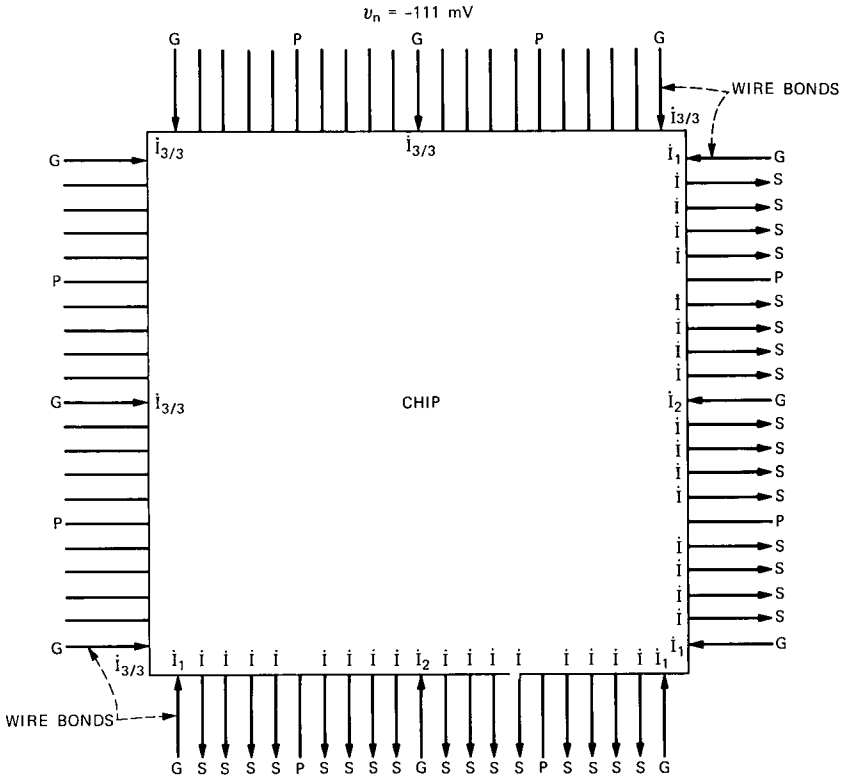


Fig. 7—Driver circuits on integrated circuit chip switching 32 signal bits simultaneously, with $v_n = -111$ mV.

solving these three simultaneous equations, we can determine $\dot{I}_3$ and from eq. (43) we can determine the inductive noise voltage, $v_n$, across the grounded wire bonds. If $\ell = 0.1$ inch, $\Delta = 0.02$ inch, $\rho = 0.0005$ inch, and $\dot{I} = 20$ mA/ns, the results are

$$L_s = 2.623 \text{ nh}$$

$$\dot{I}_3 = -6.368\dot{I} \text{ mA/ns}$$

$$v_n = -111.4 \text{ mV}. \tag{44}$$

Thus, from the inductive noise point of view, the configurations shown in Figs. 6 and 7 are comparable.

In a similar manner, one can compute the inductive noise voltage across the common power or ground leads of an arbitrary array of conductors.

In general, the inductive noise voltage, $v_n$, is linear in the switching current rate, $\dot{I}$. Thus, if $\dot{I} = 10$ mA/ns, $v_n$ as given by eqs. (40) and (44) would decrease by a factor of two. Accordingly, it is very important to keep $\dot{I}$ as small as is necessary for proper circuit operation.

Also, eq. (39) shows that the self-inductance, $L_s$, of the wire bonds is a major contributor to the inductive noise, $v_n$. Equation (12) shows that $L_s$ can be reduced by reducing the length, $\ell$, of the wire bonds or increasing its radius, $\rho$.

Notice that if all the mutual inductances were to vanish, the inductive noise voltages across the grounded wire bonds of Fig. 6 and 7 would increase in magnitude to

$$v_n = -\frac{L_s(32\dot{I})}{N_g} = -\frac{L_s(32\dot{I})}{12} = -140.0 \text{ mV}, \tag{45}$$

where $N_g$ = number of chip grounds.

Thus, in these cases, the mutual inductances serve to reduce the magnitude of inductive noise by about 20 percent.

#### *5.2.3 Minimization of inductive noise*

To help minimize the magnitude of inductive noise, two general rules are now apparent:

1. Separate the P leads, and separate the G leads. Attempt to locate them symmetrically. This serves to minimize the buildup of flux linkages produced by current flow in the same direction and provides symmetry for the P/G leads.
2. Locate the signal leads as close as possible to the P/G leads. This serves to reduce flux linkages produced by current flow in opposite directions.

Similar rules were also given by C. W. Deisch.[1]

These two rules were applied to determine the P/G/S lead assignments for Fig. 8, which shows $\min|v_n \leq 110$ mV. In contrast, the rules were violated drastically in Fig. 9 with the result that $\max|v_n| \geq 196$ mV. By comparison with eq. (45), we see that the mutual inductances have now increased the magnitude of the inductive noise by at least 40 percent.

The two simple rules are useful to help minimize inductive noise resulting from general arrays of coupled conductors.

#### *5.2.4 Comparison with experiment*

Values of $v_m$, $v_n$ as given by eqs. (24) and (26) were found to agree well with experimental values of inductive noise voltage measured on

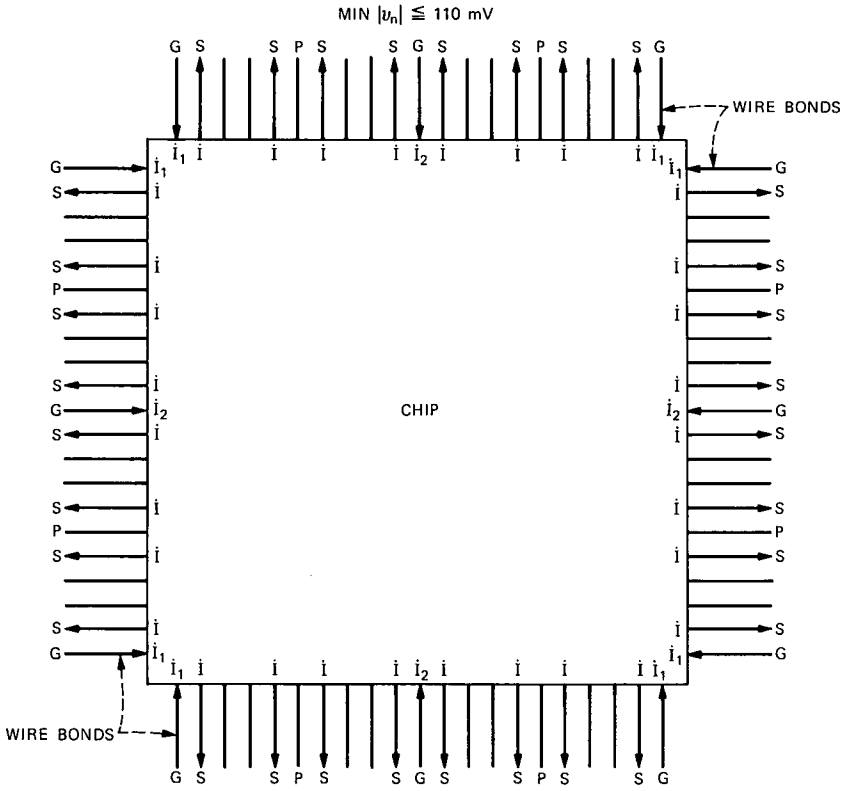


Fig. 8—Driver circuits on integrated circuit chip switching 32 signal bits simultaneously, with $\min|v_n| \leq 110$ mV.

arrays of conductors in a 4 by 10 section of a circuit-pack connector.[5,6] Details are presented in the Appendix.

### *5.2.5 Some generalizations*

When the array of conductors contains nonparallel conductors, eq. (52) of Ref. 3 can be used to generalize eq. (4) above. Also, for more general configurations of parallel conductors, eq. (28) of Ref. 3 generalizes eq. (4) above. These generalizations, along with the associated self-inductances, can also be used in eq. (26) or (28) to compute inductive noise voltage.

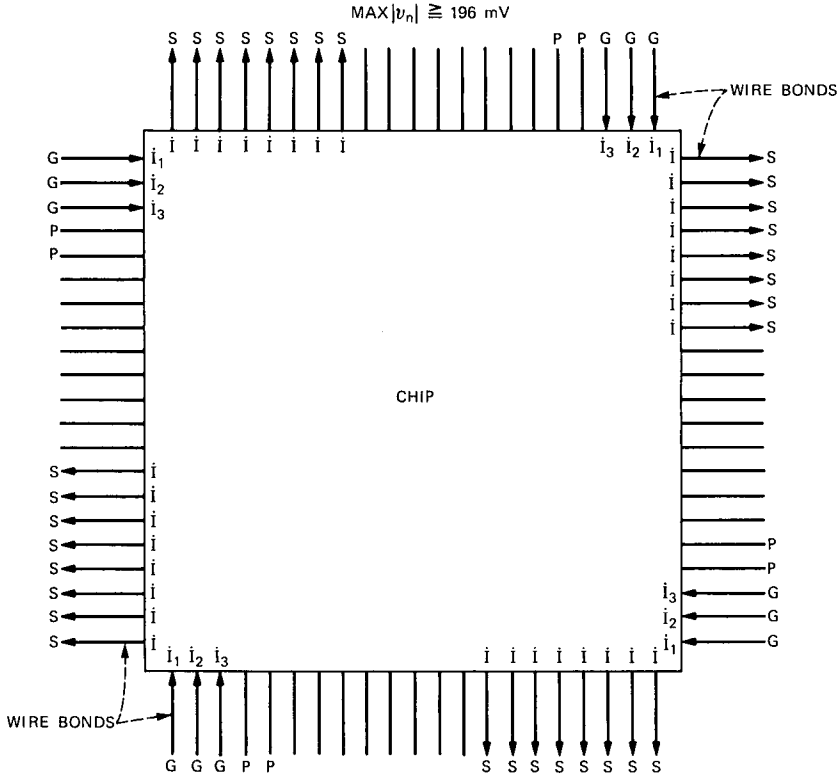


Fig. 9—Driver circuits on integrated circuit chip switching 32 signal bits simultaneously, with max$|v_n| \geq 196$ mV.

### *5.3 Power and ground planes*

The inductive noise voltage, $v_n$, in a power or ground plane can be computed from eq. (20). If the time rate of change of the current flowing in the power and ground plane is $\dot{I}_0$ mA/ns, the inductive noise voltage in either the power or ground plane is given by

$$v_n = \dot{I}_0 L_g = 5\pi \dot{I}_0 \ell \left(\frac{h}{W}\right) \text{ mV}, \tag{46}$$

where $\ell$ is expressed in inches. For example, if $\ell = 1$ inch, $W = 1$ inch, $h = 0.005$ inch, and $\dot{I}_0 = 200$ mA/ns, then $v_n = 15.7$ mV.

## VI. IMPEDANCE MATCH OF CHIP PACKAGES AND CIRCUIT PACKS

The computation of inductive noise as discussed in this paper applies when the array of conductors is considered as lumped electrical elements. This is the case for the electrically short power and ground leads and electrically short segments of signal leads. However, for electrically long signal leads, a transmission line point of view is more appropriate. In this case, an important consideration is the design of chip packages having signal leads that are impedance matched to the signal leads in a circuit pack. The impedance matching of chip packages to circuit packs was treated in Ref. 7.

## VII. CONCLUSIONS

Inductive noise limits the physical design of high-speed, high pin-out chip packages. The general eqs. (26) and (28) derived in this paper are useful for computing the inductive noise resulting from the interconnections in high-speed, high pin-out chip packages. When the distances between conductors are small relative to conductor lengths, the general equations reduce to the approximate equations given as eqs. (29) and (30). The equations are useful for computing inductive noise in general arrays of wire bonds, solder balls, DIP leads, package pins, and connector pins. Computed results were found to agree well with measured results. Two simple rules are presented for minimizing inductive noise. The inductive noise of P/G planes can also be computed.

## VIII. ACKNOWLEDGMENTS

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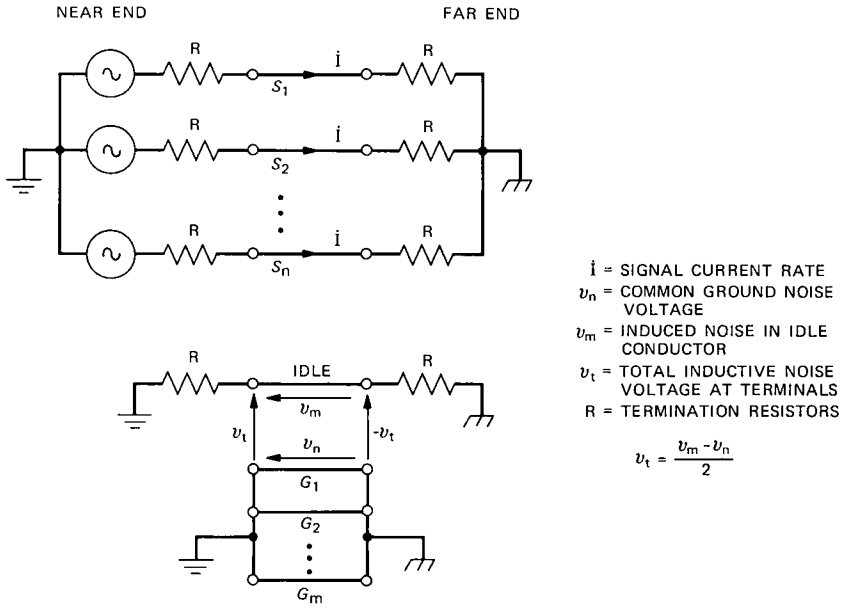


Fig. 10—Inductive noise model for an array of signal ($S_i$), ground ($G_i$), and idle conductors.

## APPENDIX

### *Experimental and Computed Inductive Noise of Interconnections*

To compare computed results with experimental results, some inductive noise measurements were made on arrays of conductors in a 4 by 10 section of a circuit-pack connector.[5,6]

A general electrical model for an array of signal ($S_i$), ground ($G_i$), and idle conductors is shown in Fig. 10. The signal leads ($S_i$) are assumed to carry current rates $\dot{I}$, which occur simultaneously. The voltages $v_t$, $v_n$, and $v_m$ are used to characterize the inductive noise induced in the closed circuit loops. The two different ground potentials represent two equipotential surfaces (i.e., two copper ground planes).

The measurements were performed for the four grounding patterns shown in Fig. 11. The percentage of grounds varies from 50 percent for ground pattern I to 10 percent for ground pattern IV.

The experimental results for $v_t$ are presented in Table II, along with the corresponding computed results for the case of a signal rise time of 6 ns and termination resistors of 100Ω. The physical dimensions used were obtained by measurements on the circuit-pack connector.[5,6]

The entries labeled single refer to the case when the average radius (with respect to length) is taken as 0.0234 inch and the total conductor length is taken as 0.790 inch.

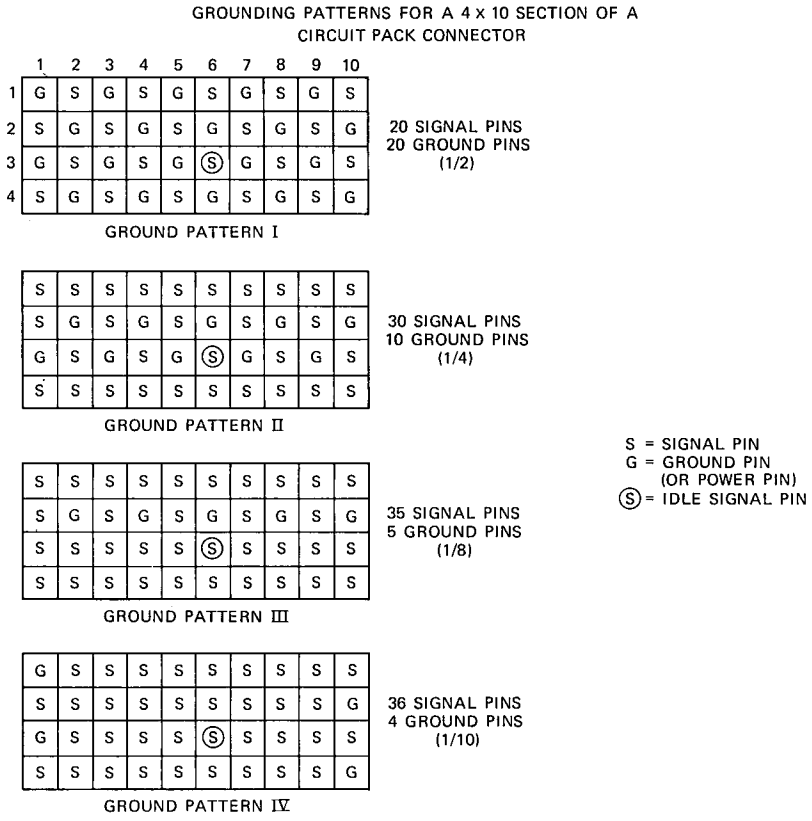


Fig. 11—Grounding patterns I, II, III, and IV.

Table II—Comparison of experimental and computed inductive noise with $T_R = 6$ ns, $R = 100\Omega$

| Pattern | Percent $v_t$ (Experimental) | Percent $v_n$ | Percent $v_m$ | Percent $v_t$ (Computed) | |
|---|---|---|---|---|---|
| I | 0.3 | −0.889 | −0.481 | 0.204 | Single |
| | | −0.917 | −0.429 | 0.244 | Cascade |
| | | −0.976 | −0.492 | 0.242 | Joint |
| II | 0.9 | −4.46 | −2.34 | 1.06 | Single |
| | | −4.21 | −1.91 | 1.15 | Cascade |
| | | −4.73 | −2.36 | 1.19 | Joint |
| III | 4.0 | −9.88 | −1.18 | 4.35 | Single |
| | | −9.46 | −0.943 | 4.26 | Cascade |
| | | −10.51 | −1.19 | 4.66 | Joint |
| IV | 9.0 | −13.83 | +9.24 | 11.54 | Single |
| | | −13.23 | +6.63 | 9.93 | Cascade |
| | | −14.64 | +9.24 | 11.94 | Joint |

The entries labeled "cascade" refer to the case when the $v_t$'s for two subsections of each conductor were added. The first subsection represents a radius of 0.015 inch and a length of 0.5 inch. The remaining subsection was of radius 0.038 inch and of length 0.290 inch.

Finally, the entries labeled "joint" refer to the case when a single $v_t$ was evaluated for each conductor having the radii and lengths given in the previous paragraph.

By comparing the experimental values of $v_t$ in Table II with the corresponding triplet of computed values, we see that there is indeed good agreement in all cases.

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